TRS-3

(1)

Technical Reliability Studies

EOS/ESD TECHNOLOGY ABSTRACTS

Winter 80-81

RAC

Reliability Analysis Center

ROME AIR DEVELOPMENT CENTER

THE RELIABILITY ANALYSIS CENTER IS A DOD INFORMATION ANALYSIS CENTER

Reliability Analysis Center

A DoD Information Analysis Center

Technical Reliability Studies

EOS/ESD TECHNOLOGY ABSTRACTS

Winter 80-81

Prepared by:

Eugene Kraeger
Wayne Grimaldi
IIT Research Institute

Under Contract to:

Rome Air Development Center
Griffiss AFB, NY 13441

Ordering No. TRS-3

The RELIABILITY ANALYSIS CENTER is a DoD Information Analysis Center, operated by IIT Research Institute under contract to the Rome Air Development Center, AFSC.

The Reliability Analysis Center (RAC) is a Department of Defense Information Analysis Center sponsored by the Defense Logistics Agency, managed by the Rome Air Development Center (RADC), and operated at RADC by IIT Research Institute (IITRI). RAC is charged with the collection, analysis and dissemination of reliability information pertaining to parts used in electronic systems. The present scope includes integrated circuits, hybrids, discrete transistors and diodes, microwave devices, optoelectronics, and selected nonelectronic parts employed in military, space and commercial applications.

In addition, a System/Equipment Reliability Corporate Memory (RCM) is also operating under the auspices of the RAC and serves as the focal point for the collection and analysis of all reliability-related information and data on operating and planned military systems and equipment.

Data are collected on a continuous basis from a broad range of sources including testing laboratories, device and equipment manufacturers, government laboratories, and equipment users, both government and nongovernment. Automatic distribution lists, voluntary data submittal, and field failure reporting systems supplement an intensive data solicitation program.

Reliability data documents covering most of the device types mentioned above are available annually from RAC. Also, RAC provides reliability consulting and technical and bibliographic inquiry services which are fully discussed at the end of this document.

REQUESTS FOR TECHNICAL ASSISTANCE AND INFORMATION ON AVAILABLE RAC SERVICES AND PUBLICATIONS MAY BE DIRECTED TO:

Charles E. Ehrenfried
Reliability Analysis Center
Rome Air Development Center (RBRAC)
Griffiss Air Force Base, NY 13441
Telephone: 315/330-4151
Autovon: 587-4151

ALL OTHER REQUESTS SHOULD BE DIRECTED TO:

Rome Air Development Center
RBE/Charles F. Bough
Griffiss Air Force Base, NY 13441
Telephone: 315/330-4920
Autovon: 587-4920

PREFACE

The purpose of this bibliography is to make more accessible present information on Electrical Overstress and Electrostatic Discharge. Duplication of previous studies can be avoided by the increased information retrieval capability provided by this bibliography.

TABLE OF CONTENTS

INTRODUCTION AND USER'S GUIDE

The EOS/ESD Technology Abstracts references literature pertinent to Electrical Overstress and Electrostatic Discharge damage or degradation of electronic devices. Aspects ~~found herein~~ encompass design, failure analysis, protective measures and techniques, and training programs. References are selected for citation from the Reliability Analysis Center document files. The portion presented here dates from acquisitions made during 1969 to February 1980. Documents are selected on the basis of informational currency and usefulness as well as availability to the engineering community.

ARRANGEMENT

This publication is arranged in eight sections: alphabetical list of terms (subjects), (subject) index, author index, corporate index, keywords in title index, source index, technology abstracts, and standards.

The **ALPHABETICAL LIST OF TERMS** is a list of terms without citations and serves as a look-up table for the "index" which it precedes. The terms are arranged alphabetically to permit easy scanning for selecting similar terms. Scanning of this list can have the following useful benefits: (1) the researcher can develop a search strategy by serendipitous association and (2) the likelihood of overlooking a highly relevant citation is minimized.

The **INDEX** is the alphabetical list of terms of Section 1 with citations. The citations include the document number and the title of the documents. Including the title is a convenience which provides a possibility for selecting the most appropriate citation and eliminating those not applicable without the necessity of looking up more information elsewhere.

The **AUTHOR INDEX** is an alphabetical list of all authors cited whether principal or secondary.

The **CORPORATE INDEX** is an alphabetical list of all corporations, companies, institutions and government agencies with whom the authors were affiliated at the time the papers were prepared. Citations in the index include document number and title.

The **KEYWORD IN TITLE INDEX** is an alphabetical list of selected keywords in the title of the documents. Citations include document number and title. This index can be used to locate documents for which the keyword is a principal topic.

The **SOURCE INDEX** is an alphabetical list of the sources where the documents may be obtained.

The **TECHNOLOGY ABSTRACTS** provide complete coverage of the citations. Abstracts are in ascending numeric order.

The **STANDARDS** provide a list of government and industry standards.

IMPLEMENTATION

These indexes were composed and printed out on RADC's Honeywell 6180 computer using the General Comprehensive Operating Systems (GCOS). Programs for data input and the output reports were developed by RAC software engineers. The final manuscript was printed on an Anderson-Jacobson (Model AJ832) terminal.

SEARCH EXAMPLE

The following example illustrates the use of Section I and II:

Suppose we are interested in studying the input protection on CMOS devices. The possible terms for finding applicable citations, we decide, would be "CMOS," "Input" and "Protection." Scanning Section I for these terms, we find by serendipitous association the following terms listed:

CMOS B Series Versus A Series Input Protection
CMOS Devices
CMOS Protection Levels
Input Protection
Protection Networks
Protection Techniques

When the terms are looked up in the index (Section II), the following ten citations are accepted for study:

10395	13717
12309	13720
13309	14075
13310	14983
13672	16067

HOW TO OBTAIN DOCUMENTS IN THIS BIBLIOGRAPHY

Each reference listed herein contains complete bibliographic information including the personal and corporate author with location. Where the document is available from one of the government document distribution centers, see information shown below. Other documents can be obtained from the original source (i.e., author, journal, society, etc.). **Documents other than those published by RAC cannot be obtained from RAC.**

To determine the availability of government documents write or phone:

National Technical Information Service
(NTIS)
5285 Port Royal Road
Springfield, Virginia 22151
(703)321-8888

or if you are a government contractor, contact:

Defense Technical Information Center
(DTIC)
Cameron Station
Alexandria, Virginia 22314
(202)694-7633

SECTION 1

ALPHABETICAL LISTING OF INDEX TERMS

ALPHABETICAL LISTING OF INDEX TERMS

ALPHABETICAL LISTING OF INDEX TERMS

SECTION 2

INDEX

INDEX

INDEX

INDEX

INDEX

INDEX

INDEX

INDEX

INDEX

INDEX

INDEX

INDEX

INDEX

INDEX

SECTION 3

AUTHOR INDEX

AUTHOR INDEX

AUTHOR INDEX

AUTHOR INDEX

AUTHOR INDEX

DERMARDEROSIAN, A.

16147 THE GENERATION OF ELECTROSTATIC CHARGES IN SILICONE ENCAPSULANTS DURING CYCLIC GASEOUS PRESSURE TESTS

DI CIACCIO, C.

15092 CMOS INTEGRATED CIRCUIT
15091 40 PIN PMOS INTEGRATED CIRCUIT

DICKEN, H.K.

14905 INTEGRATED CIRCUIT FAILURE MODES

DODSON, G.A.

16157 THE PHANTOM EMITTER - AN ESD-RESISTANT BIPOLAR TRANSISTOR DESIGN AND ITS APPLICATIONS TO LINEAR INTEGRATED CIRCUITS
13718 EFFECTS OF ELECTROSTATIC DISCHARGE ON LINEAR BIPOLAR INTEGRATED CIRCUITS

DOHM, D.L.

11885 RELIABILITY ANALYSIS OF MICROCIRCUITS FAILURES IN AVIONIC SYSTEMS (RAMFAS)

DOMINGOS, H.

16204 SQUARE PULSE AND RF PULSE OVERSTRESSING OF UHF TRANSISTORS

DOMINICK, F.

12351 HOW MUCH PULSED POWER CAN A PIN DIODE HANDLE?

DUNCAN, D.E.

16285 USERS MANUAL FOR SUPERSAP2

DUNN, R.

13672 INPUT PROTECTION NETWORKS ON MOS DEVICES

DURGIN, D.L.

14026 ELECTROMAGNETIC SUSCEPTIBILITY OF SEMICONDUCTOR COMPONENTS

EBEL, G.H.

10379 FAILURE ANALYSIS OF OXIDE DEFECTS

EICHEL, F.G.

14960 ELECTROSTATICS

ELLISOR, R.W.

17079 CONTROL OF ELECTROSTATIC INTERFERENCE IN SPACECRAFT

ENGELKE, H.A.

10379 FAILURE ANALYSIS OF OXIDE DEFECTS

ENOCH, A.F.

15002 ELECTROSTATIC DISCHARGE DAMAGE PREVENTION

ERICKSON, D.

14975 ANTISTATIC EQUIPMENT AND TECHNIQUES

FORMANEK, V.C.

16377 EMP TO ESD VZAP DATA CONVERSION AND CONSIDERATIONS
161[illegible]1 DAMAGE RESPONSE OF SELECTED INTERFACE INTEGRATED CIRCUITS TO A SIMULATED EMP WAVEFORM

FRANKEL, H.C.

14646 THICK FILM RESISTOR ELECTROSTATIC VULNERABILITY TEST STUDY

AUTHOR INDEX

SECTION 4

CORPORATE ISSUES

CORPORATE INDEX

CORPORATE INDEX

CORPORATE INDEX

CORPORATE INDEX

SECTION 5

KEYWORDS IN TITLE INDEX

SECTION 6

SOURCE INDEX

INDEX

INDEX

INDEX

SECTION 7

TECHNOLOGY ABSTRACTS

01823

Klein, N. (Bell Telephone Laboratories, Allentown, PA)
ELECTRICAL BREAKDOWN IN THIN DIELECTRIC FILMS.
Solid State Science, Vol. 116, No. 7, pp. 963-972, July 1969.

Thermal and electric breakdown processes in thin film insulators are discussed. Interpretation of the processes is greatly facilitated by using specimens with self-healing breakdowns cleared of weak spots. Electric breakdown can be initiated by the increase of the electrical conductance in a channel by a pulse, such as an electronic avalanche. Breakdowns occur at a rate which increases quasi-exponentially with field and also with temperature.

02101

HO, R. (American Electronic Laboratories, Colnar, PA)
ELECTROSTATIC EFFECTS ON FILM RESISTORS.
Insulation/Circuits, Vol. 17, No. 4, pp. 33-36, April 1971.

Static electricity has the most pronounced effect on thick film resistors smaller than 40 mils square having a sheet resistivity of several thousand ohms. Electrical conductivity is from each semiconductor particle in the glass matrix to another. Electrostatic discharge will rupture the insulation and cause the metallic islands to become part of a conductive path. This can cause a downward shift in resistance value greater than 50%. The ends of resistors are greatly affected by ESD in inverse proporation to width. Static effects can be eliminated by care in processing and humidity control.

02262

Lenzlinger, M. (Fairchild Semiconductor, Palo Alto, CA)
GATE PROTECTION OF MIS DEVICES.
IEEE Trans. on Electron Devices ED-18, no. 4, 21 pp., April 1971.

Gate shorts caused by electrical breakdown of the gate dielectric are a major yield and reliability problem for MOS transistors and integrated circuits. Diodes or diffused resistors with breakdown voltages of about 40V can be used to protect the gate from high voltage transients or static discharges. This paper provides a uniform approach to gate protection.

04783

Smith, J.S. (RADC, Griffiss AFB, NY)
PULSE POWER TESTING OF MICROCIRCUITS.
Rept. No. RADC-TR-71-59, 50 pp., October 1971.

Failure analysis of microcircuits subjected to high current transient pulses shows the principal cause of failure to be junction shorting. Thin film resistors are especially susceptible. Current and thermal profile analyses do predict the required energy to cause burnout. Metallization burnout is a function of current density for 200 nsec pulses but depends more on the thickness of the SiO_2 passivation at longer pulse widths.

04834

Lane, C.H. (RADC, Air Force Systems Command, Griffiss AFB, NY)
ELECTRICAL OVERSTRESS FAILURES IN SILICON DEVICES.
Rept. No. RADC-TR-72-148, 36 pp., July 1972.

Experimental evidence is used to substantiate a proposed mechanism of overstress failures. The mechanism is considered to be a migration of liquid along a line determined by crystal and electric fields. Graphs are given showing the relationship between voltage and electrode spacing. Oxidation temperature is identified as a factor that affects sensitivity, higher temperature oxidation providing devices with higher resistance to surface zaps.

10342

Van Beek, H.W. (Texas Instruments Inc., Houston, Texas)
MOS/LSI CIRCUIT DESIGN: DESIGNING-IN RELIABILITY.
IEEE - 10th Reliability Physics Symposium, pp. 36-41, 1972.

The solution to the need for extensive burn-in and temperature cycling calls for the circuit designer to "design-in" product reliability. By "designing-in reliability" is meant establishing reliability by design and fabrication with appropriate experimental monitoring. This is not a novel concept by any means but all too often it is forgotten when the topic of reliability is discussed. The application of this concept in MOS circuit design requires an understanding of the tools available to the designer and their relative importance and how they affect the MOS circuit design.

10379

Ebel, G.H., Engelke, H.A. (Singer-Kearfott Division, Wayne, NJ)
FAILURE ANALYSIS OF OXIDE DEFECTS.
IEEE - 11th Reliability Physics Symposium, Catalog No. 73 CHO 755-9-PHY, pp. 108-116, 1973.

There have been many good papers presented on various failure analysis techniques for studying oxide defects. This paper will review some of these and will describe, in detail, the application of nematic liquid crystals to the problem of locating the failure sites in oxides.

10395

Linholm, L.W. (National Security Agency, Ft. George C. Meade, MD) and Plachy, R.F. (Johns Hopkins University, Silver Springs, MD)
ELECTROSTATIC GATE PROTECTION USING AN ARC GAP DEVICE.
IEEE - 11th Reliability Physics Symposium, pp. 198-202, 1973.

An ideal MOS protection device should respond to very fast and very slow rise time pulses and be able to short the input to ground before damage to the gate can occur. In general, all failures occur where the gate oxide overlaps the source or drain. The field plate protective diode by itself affords no protection to fast rise time pulses because of its connection in parallel with the input gate.

An arc gap is formed by locating the bonding pad 2.0 mils from a ground metallization ring encircling the chip. The ambient package atmosphere will support a low impedance gaseous discharge from pad to ground ring. No other metallization should be located within 2 mils of the bonding pad, and the area should not be passivated from the ambient air.

10599

Tasca, D.M., Pedan, J.C., Andrews, J.L. (General Electric)
THEORETICAL AND EXPERIMENTAL STUDIES OF SEMICONDUCTOR DEVICE DEGRADATION DUE TO HIGH POWER ELECTRICAL TRANSIENTS.
Rept. No., 73SD4289, Contract No. DAAG39-72C-0066, December 1973.

The principal areas of investigation were the detailed characterization of the degradation and failure mechanisms in selected discrete, bipolar, unipolar and integrated circuit devices. A major area of interest was to show experimentally the utility of square wave pulsed-power damage testing in the prediction of semiconductor device response for complex power waveforms typical of electromagnetic pulse (EMP) induced transients.

The experimental program consisted of a variety of electrical damage experiments on the following device types: 1N4148 diodes, 2N918 transistors, SN5405 microcircuits, MEM806A MOSFET's and RD211 microcircuits. The pulse widths ranged from three nanoseconds to thirty microseconds.

The theoretical modeling included considerable effort in further refinement of the thermal damage models. The application of these thermal damage models derived from the square wave data was then extended to the prediction of damage to more complex waveforms. This was done through the application of Duhamel's Theorem of linear heat transfer by which one can predict the temperature rise in the body for a constant rate of heat production. Duhamel's Theorem was successfully applied for damage prediction of both unipolarity and bipolarity complex electrical waveforms based upon the knowledge obtained for damage under square wave (constant rate) pulsing.

10792

Kennan, W.F., Smith, D.M. (Texas Instruments Inc., Dallas, Texas)
PULSE POWER STUDIES OF HARDENED MICROCIRCUITS
Rept. No. RADC-TR-73-367, Contract No. F30602-72-C-0077, 77 pp., December 1973.

The effects of large amplitude transient pulses on radiation tolerant integrated circuits was investigated. Two distinct burnout mechanisms were discovered to exist, diode failure and resistor burnout. Both mechanisms were investigated independently by test structures to measure the influence of processing variations on the failure levels.

10839

Viele, A.A. (IBM, Manassas, VA)
A FAILURE ANALYSIS TECHNIQUE FOR LOCATING THE FAIL SITE IN MOSFET (LSI) LOGIC CHIPS WITH SPUTTERED SILICON DIOXIDE PASSIVATION.
IEEE - 12th Reliability Physics Symposium, pp. 16-21, 1974.

Failure analysis of MOSFET chips with sputtered SiO_2 passivation must be precluded by the removal of the passivation layer to allow probe contact. The electrical integrity of the chip must be maintained to locate the fail site by signal tracing. Mechanical removal of the SiO_2 passivation has a greater success. The chip is removed from the C-DIP by melting the eutectic or by polishing away the backside ceramic. Chips are removed from ceramic controlled-collapse connection (C-4) packages by etching the solder pads in a 5:1 solution of acetic acid/hydrogen peroxide, then rinsed in DI water, or as recommended mechanically by cutting the C4 pads on all sides of the chip. Parallel polishing in a syntron vibromat using a slurry of aluminum oxide powder (.05 micron) and DI water down to the aluminum surface removes the SiO_2. Even polishing can be facilitated by coating areas of excess polishing with fingernail polish. Electrical analysis isolates the failed circuits and signal analysis characterizes the failure mechanism. Physical analysis confirms the damage location.

10841

Gajda. J.J. (IBM System Products Division East Fishkill Facility, Hopewell Junction, NY)
TECHNIQUES IN FAILURE ANALYSIS OF MOS DEVICES
IEEE - 12th Reliability Physics Symposium, pp. 30-37.

Failure analysis of gate oxides of MOSFET devices is discussed using a copper decoration and plating technique. Static discharge failures can be readily identified while subtle gate failure (submicron) from leakage and stress testing shorts require copper decoration to identify the physical appearance of the defect site. Solutions of NH_4F(40%, 4 parts) HF(48%, 1 part) and glycerine (2 parts) are used to remove glass passivation layers; also HNO_3 (70%, 1 part) HF (48%, 5 parts) and glycerine (10 parts). Lands are opened using capacitive discharge. Aluminum is etched away using a standard H_2PO_4 - HNO_3 - CH_3COOH-H_2O solution. Polysilicon gates are removed using an etch of 20 parts HNO_3 and 1 part HF. A displacement solution of 2% $CuSO_4$ and 28% HF with a high intensity lamp locates conductive paths through the gate oxide and where gate silicon is exposed. Regions of defects are analyzed using SEM analysis. To avoid etching any oxide a standard electroplating solution of $CuSO_4$ and H_2SO_4 can be used. Pinholes in oxides, surface pits in gate region, Al_2O_3 formation in gates, single mounds and raised plateaus on oxide surface can be detected.

10843

Jones, W.K. (Charles Stark Draper Laboratory, Cambridge, MA)
PLASMA ETCHING AS APPLIED TO FAILURE ANALYSIS.
IEEE - 12th Reliability Physics Symposium, pp. 43-47, 1974.

Failure analysis is discussed using a carbon tetraflouride plasma etch. The CF_4 is excited to plasma by RF energy in a vacuum of .7 torr. Helium is used to control the reaction as it is viewed through a sapphire viewer under a stereomicroscope @ 150x magnification. Prior to complete removal the subpassivation aluminum has a green yellow tint, while bonding pad metallization is metallic in appearance. Backgrinding and polishing with final plasma etch will reveal the underside of metallization.

Examples given of the use of optically controlled plasma etching are: (1) removal of passivation for SEM analysis; (2) backlapping of bipolar devices; (3) thin-section for TEM analysis of nichrome fuses.

10845

Speakman, T.S. (Western Electric Company, Inc. Reading, PA)
A MODEL FOR THE FAILURE OF BIPOLAR SILICON INTEGRATED CIRCUITS SUBJECTED TO ELECTROSTATIC DISCHARGE.
IEEE - 12th Reliability Physics Symposium, pp. 60-69, 1974.

A mathematical model to predict ESD voltage thresholds is presented. Device failure occurs as a result of emitter-base junction degradation caused by electrical overstress. The degradation is manifested as a lowered breakdown voltage or higher reverse leakage current. The charges may come from a human body or the device itself. The resulting current of discharge is an exponentially decaying pulse. The failure is deemed to have occurred when the local power density causes the temperature to melt the semiconductor. The threshold level is a function of the current path cross section area, not of the junction area. The total power dissipated is the expression $P=V_Di + R_Bi^2$ (V_D = junction drop and R_B = junction resistance). The current path is from the edge of the emitter to the base contact. Its area is emitter length times base junction depth. The power density vs pulse length is plotted to show good correlation with the Wunsch-Bell plot.

10873

Freeman, E.R., Beall, J.R. (Martin Marietta Corp., Denver, CO)
CONTROL OF ELECTROSTATIC DISCHARGE DAMAGE TO SEMICONDUCTORS.
IEEE - 12th Reliability Physics Symposium, pp. 304-312, 1974.

A study was done on the failures of three devices. The first, a 2N3970 N-channel FET, suffered a degraded reverse breakdown when subjected to ESD pulses of 6000v. The second, a 2600 internally compensated amplifier, suffered a shorted MOS compensation capacitor when subjected to ESD pulses. The third example, a 54L04 hex inverter low power TTL circuit, experienced phase-splitter transistor failure mode subjected to ESD pulses of 2500 to 3000v. Facilities were examined and verified the presence of electro-static charges in excess of the levels necessary to produce failures in the laboratory.

10993

Himmel, R.P. (Hughes Aircraft, Culver City, CA)
THE EFFECT OF STATIC ELECTRICITY ON THICK FILM RESISTORS.
Insulation/Circuits, pp. 41-44, September 1972.

The effects of static electricity in the manufacturing process, packaging and use of thick film resistors is analyzed. Thick film resistors' sensitivities are related to resistivity which in turn is directly related to the materials used in manufacture. Isolated metal particles take part in the conduction process through the breakdown of dielectrics between particles. The clean room conditions of manufacturing often result in high static charge levels. Elimination of these charges may be facilitated by special precautions. The use of protective packaging materials is encouraged.

11207

Whelan, C.D. (RCA, Somerville, NJ)
RELIABILITY EVALUATION OF C/MOS TECHNOLOGY IN COMPLEX INTEGRATED CIRCUITS.
Rept. No. RADC-TR-C-0282, 210 pp., March 1976.

The objective of this study was to investigate reliability of small and medium scale CMOS integrated circuits. Four manufacturers' type 4011A Quad 2-input NAND gates and three manufacturers' type 4015A dual four stage static shift registers were chosen as test vehicles. Only Manufacturer A's product was intended for MIL-M-38510 end use.

11295

Vandre, R.H. (Aerospace Corp., Technology Division, El Segundo, CA)
PULSE-POWER BURNOUT OF INTEGRATED CIRCUITS.
Rept. No. TR-0073 (3124)-1, SAMSO-TR-72-226, Contract No. F04701-72-C-0073, 33 pp., August 15, 1972.

Results of pulsed power burnout testing of the Fairchild 9046 quad dual-input NAND gate and the Amelco 6041 three input NAND gate showed the circuits to be vulnerable to junction burnout for pulses of less than 100v and pulse widths on the order of 100 nsec. Calculations based on Wunsch-Bell junction burnout theory showed good agreement with experimental results. Sample calculations are given.

11436

Yang, D.Y., Johnson, W.C., Lampert, M.A. (Princeton University, Princeton, NJ)
A STUDY OF THE DIELECTRIC BREAKDOWN OF THERMALLY GROWN SILICON DIOXIDE BY THE SELF-QUENCHING TECHNIQUE.
IEEE - 13th Reliability Physics Symposium, pp. 10-14, 1975.

The dielectric breakdown of SiO_2 is studied using a thin metallization. The dielectric breakdown results in removal of metallization in the area of breakdown. Positive plate voltages resulted in anisotropic removal of metallization regardless of silicon dopant. Negative plate voltages result in irregular metallization removal. With positive field plate potentials and p-type substrate the anisotropic breakdown regions were square with smooth edges. The anisotrophy is explained by hot electron conduction in the presence of a large radial electric field. Slow-high field instability also resulted in Al-SiO_2 structural breakdown enhanced at lowered temperatures. A steady state current was observed and attributed to the tunneling of electrons in the presence of field plate voltages well below the point of instability. The instability results when the production and trapping of holes dominates over recombination caused by electron tunneling from the silicon substrate into the conduction band of the oxide.

11494

Hampel, D. (RCA, Advanced Communications Laboratory, Somerville, NJ)
EMP HARDENED CMOS CIRCUITS.
Rept. No. HDL-TR-192-1, Code No. 691000.22.63516, Contract No. DAAG39-73-C-0136, 35 pp., October 1973.

This paper shows how CMOS integrated circuits can be protected against electrical transients originating from nuclear explosions, static discharge, etc. First, the causes of transient failures are determined and then analyzed. Next, a wide range of protection devices are designed and evaluated. Finally, complete transient hardened logic gates are fabricated and tested to prove the feasibility of EMP hardened CMOS circuits.

11704

Kirk, W.J., Carter, L.S., Waddell, M.L. (Bendix, Kansas City Division, Kansas City, MO)
CONTROL OF ELECTROSTATIC DAMAGE TO SOLID STATE DEVICES.
Contract No. AT(29-1)-613 USAEC, Rept. No. BDX-613-1080, March 1974.

The control and elimination of static discharge in the work area is discussed. The human body is represented in a capacitive discharge model. The degradation to a 2N4118A varies according to the resistance in series with the human discharge. A transient voltage detection system is used to monitor ESD. The peak voltages generated by operators occurred when an operator lifts her feet or increases the static charge by gliding in a rollered chair. Conductive shoes on a conductive floor can limit static voltages to as low as 50 volts. Increased relative humidity above 45% can also reduce static levels. Spray cleaning increases the electrostatic potential. Wrist straps are shown to be impractical. Conductive floor, chair and shoes all help to reduce static voltages as do conductive packaging, table tops and grounded soldering tips.

11885

Dohm, D.L., McCammack, R.J., Utz, T.E. (McDonnell Douglas Corp., McDonnell Aircraft Co., St. Louis, MO)
RELIABILITY ANALYSIS OF MICROCIRCUIT FAILURES IN AVIONIC SYSTEMS (RAMFAS).
Rept. No. RADC-TR-76-3, Vol. I - Tech. Rept., AD/A021 428, Vol. II - Appendices, F30602-74-C-0319, June 1975.

The report documents the analysis of 308 devices out of 438 microcircuit removals from 31,393 microcircuits assembled, tested and shipped to the field in 39 HUD and 35 IBS. Only one identified field failure occurred in 4.537 x 10^6 microcircuit hours and provided a measured microcircuit failure rate of 0.22%/1000 hours for the combined HUD-IBS equipment as compared to the .1335%/1000 hours predicted microcircuit failure rate via RADC-TR-67-108 stress analysis methods. No new or unique microcircuit failure modes/mechanisms were reported. Two sense amp failures were attributed to ESD. Over 40 EOS failures of 741 op amps were found.

11926

Hewitt, H.J., Blore, R.A. (RADC, Griffiss AFB, NY) and Whalen, J.J. (SUNY at Buffalo)

SUSCEPTIBILITY OF UHF RF TRANSISTORS TO HIGH POWER UHF SIGNALS - PART II.
Rept. No. RADC-TR-76-44, Contract No. F30602-75-C-0122, 74 pp., April 1976.

The electromagnetic vulnerability data needed to determine the effects of high power microwave signals on solid state components involves testing 2N5179 and 2N918 transistors using 240mhz RF single pulse signals. Physical analysis of the 2N5179 revealed emitter base shorting.

11980

Wunsch, D.C., Bell, R.R. (BDM Inc., El Paso, TX)
DETERMINATION OF THRESHOLD FAILURE LEVELS OF SEMICONDUCTOR DIODES AND TRANSISTORS DUE TO PULSE VOLTAGES.
IEEE-Transactions on Nuclear Sciences, NS-15, No. 6, pp. 244-258, December 1968.

Theoretical predictions of circuit failure in an Electromagnetic Pulse (EMP) environment require a knowledge of failure levels for each component of the circuit due to surge voltages or currents. For most circuits, the semiconductor devices are the weakest elements with respect to such failure. This paper presents the results of an extensive experimental program to determine pulse power failure levels of semiconductor junctions. Approximately 80 different types of silicon diodes and transistors were studied with variations in junction areas for 10^{-4} to 10^{-1} cm^2 and with widely varying function geometries. Power levels of up to two kilowatts, with time durations of 0.1 to 20 microseconds, were applied to semiconductor junctions in both forward and reverse polarity modes. A semi-empirical formula, based on experimental data and on a simple thermal failure model is given. From the formula one can make order-of-magnitude estimates of the failure level as a function of pulse length for many silicon diodes or transistors whose junction area is known.

12102

Hollis, R.H. (Sanders Associates)
SUMMARY OF MOS HANDLING PRECAUTIONS AND PRACTICES.
Rept. No. D5877, 1-1611-2584A, S-3A-ADP, 3 pp., September 3, 1971.

This document contains general information regarding precautions relating to the handling of MOS semiconductor devices. This summary was compiled from information obtained for other equipment manufacturers. The technical rationale for such handling precautions is not included in this report. Such information is available in the reference report files.

12227

Himmel, R.P. (Hughes Aircraft Company, Culver City, CA)
HIGH VOLTAGE SENSITIVITY OF A NEW GENERATION OF THICK-FILM RESISTOR MATERIALS.
1975 International Microelectronic Symposium, pp. 273-78, 1975.

The results of a new study into the high voltage sensitivity of this "new" generation of resistor materials is reported here. In this study, thick-film resistive pastes from five manufacturers were printed, fired, and tested for sensitivity to electrostatic discharge. The results of the tests indicate significant change from the materials previously tested, with an order of magnitude reduction in resistor sensitivity in many cases.

12278

Biddle, J.G. (Hughes Aircraft Company)
DON'T GIVE ME ANY STATIC.
Internal Report, 40 pp., 1979.

Packaging and handling precautionary measures that should be with ESD devices from Receiving to Shipping are described. Anti-static equipment needed at the work station is also identified. Advantages and disadvantages of different materials and equipment are discussed as well as the results of an evaluation on ionizing air blowers.

12309

Trigonis, A.C. (Jet Propulsion Laboratory, Pasadena, CA)
ELECTROSTATIC DISCHARGE IN MICROCIRCUITS DETECTION AND PROTECTION TECHNIQUES.
Annual Reliability and Maintainability Symposium, Contract No. NAS 7-100, January 18, 1975.

ESD failures are analyzed as to location and extent of damage using SEM and standard optical analysis. Circuit analysis and electrical probing locate the site of failure. An HA-2700 operational amplifier failed as a result of ESD punch-through causing a 400 ohm short across a MOS capacitor (another device had a 200 ohm short). The HA-2600 high impedance op amp exhibited a similar failure mode, also the HA2520 high slew rate op-amp. Bipolar microcircuits such as the LM723H exhibited electrical degradation of the input bipolar transistors as a characteristic ESD failure. No surface damage was observed by optical microscopy or SEM except in the induced current mode. Evidence of small microcracks occurred in the damaged junctions of the LM101H device. The electron beam induced current display revealed a leakage path at the crack. The failures were analyzed to be a result of ESD because of the high voltage, low energy nature of the damage.

12351

Dominick, F. (GHZ Devices, Inc., Chelmsford, MA)
HOW MUCH PULSED POWER CAN A PIN DIODE HANDLE?
Microwaves, Vol. 15, No. 2, pp. 54-59, February 1976.

A thermal analysis is necessary to determine the peak pulsed power that a PIN diode can safely switch. Thus the maximum power handling problem is thermal in nature involving heat flow analysis. For the noncontinuous or pulsed case the peak power also depends on pulse width (t_p) and pulse interval (t_r=(rep rate)$^{-1}$). Thermal time constants play an important role in the eventual cooling of the device and inital meltdown. Temperature gradients and thermal resistance are functions of device geometry, doping and the material used in mounting the device.

12439

Anon. (Tektronix, Beaverton, OR)
GUIDELINES FOR HANDLING STATIC SENSITIVE COMPONENTS.
16 pp., April 6, 1976.

Tektronix Instruments has incorporated guidelines for handling static sensitive components. Decisions should be made by the appropriate manager based on the following criteria: density of MOS static sensitive parts in the product, initial cost of devices, in-plant repair costs, warranty costs, reliability goals of the product, failure analysis indicating a static problem and cost of the static-free work station.

12502

Keenan, W.F. (Texas Instruments Inc., Dallas, TX)
PULSED OVERLOAD TOLERANCE OF SI/CR, NI/CR AND MO/SI THIN FILM RESISTORS ON INTEGRATED CIRCUITS.
IEEE - Transactions on Reliability, Vol. R-25, No. 4, pp. 248-255, October 1976.

The maximum Fusing Voltage (FV) (for 0.1-10 microsecond pulses) of Mo/Si, Ni/Cr, and Si/Cr resistors formed on oxidized Si substrates has been experimentally shown to be essentially independent of the following parameters: 1) resistive film material, 2) passivation film material (but a crack-free film is important for Ni/Cr resistors) and 3) the thickness of the oxide film between the resistor and silicon substrate (0.5-1.5 micrometer). The FV depends on the resistor geometry, substrate material, and post fabrication annealing of the resistors. The most commonly used resistor geometry is adequate for use on ICs. The most dramatic change in FV obtained in the study was for resistors formed on glass substrates. The FV was reduced by almost a factor of 2 for 0.1 microsecond pulses over that of resistors on Si substrates.

Post fabrication annealing resulted in marked increases in FV for each material for the 0.1 microsecond pulses but had diminishing effects for 1.0 and 10 microseconds. Annealing for times greater than 60 minutes or temperatures greater than 470° did not result in important further increases.

12686

Walker, R.C., Rickers, H.C. (IIT Research Institute)
SEMICONDUCTOR ELECTROSTATIC DISCHARGE DAMAGE PROTECTION.
Society of Automotive Engineers, Contract No. AF 30602-76-C-0192, Rept. No. 770228, 12 pp., 1977.

ESD is generated upon the contact of two dissimilar materials. Contact then separation results in the retention of charges. The magnitude of the charges generated depends on the ranking of materials in the triboelectric series and the intimacy and duration of contact. Fast, repetitive contact increases charge accumulation. Electronic semiconductor devices are particularly susceptible to ESD because of the catastrophic damage which results upon contact. Metal gate MOS devices are unusually susceptible. As a result of this susceptibility input protection circuitry has been devised and is successful at low limits of ESD. Failure analysis should be used whenever ESD damage is suspected. Failure duplication caused by ESD overstress can be used to confirm ESD damage. Precautionary measures to prevent ESD damage include the identification of electrostatic sources using a noncontacting electrostatic voltmeter. Grounding, humidity control, ionized air and protective clothing can all be used to eliminate the source of ESD.

12728

De La Moneda, F.H., Debar, D.E., Stuby, K.P., Bertin, C.L. (IBM, Manassas, VA)
HYBRID PROTECTIVE DEVICE FOR MOS-LSI CHIPS.
IEEE-Transaction on Parts, Hybrids, and Packaging, Vol. PHP-12, No. 3, pp. 172-175, September 1976, or ECC, pp. 103-108, 1976.

Several structures that can be used to protect MOS-LSI chips against electrostatic discharges (ESD) are examined experimentally to determine some of the possible specification tradeoffs that result in improved overall performance. It is shown that by using structures able to withstand larger energy discharges at the expense of their voltage-clamping characteristics, higher overvoltages can be handled. Additional protection is possible by incorporating a spark-gap device on the chip-carrying module. Conditions under which this hybrid combination is effective are examined.

13210

Li, S.P., Bates, E.T., Maserjian, J. (Jet Propulsion Laboratory, Pasadena, CA)
TIME-DEPENDENT MOS BREAKDOWN.
Solid-State Electronics, Vol. 19, No. 3-E, pp. 235-239, 1976.

A general model for time-dependent breakdown in metal-oxide-silicon (MOS) structures is developed and related to experimental measurements on samples deliberately comtaminated with Na. A statistical method is used for measuring the breakdown probability as a function of log time and applied field. It is shown that three time regions of breakdown can be explained respectively in terms of silicon surface defects, ion emission from the metal interface, and lateral ion diffusion at the silicon interface.

13265

Jowett, C.E.
STATIC ELECTRIFICATION HAZARDS IN MICRO-ELECTRONICS PRODUCTION.
Microelectronics and Reliability, Vol. 13, No. 6, pp. 543-547, 1974.

Three criteria exist for the existence of an electrostatic hazard: (1) charging of material or nearby structures; (2) slow, small leakage of such charge; (3) ignition, explosion, or damage by ensuing sparks of material. Relative humidity and ionization of the local atmosphere decrease the relaxation time for stored charge. Warning devices include goldleaf electroscopes, neon lamps, electro-static voltmeters, electrometers and field mills. The magnitude and polarity of the charge acquired by a powder or its container may depend on: (1) the moisture content of the atmosphere and the powder; (2) the particle size distribution; (3) the velocity with which the powder moves or impinges on surfaces; (4) the state of surfaces on which the particles impinge. Ignition of combustible gases requires a minimum spark energy and voltage.

13309

Gallace, L.J., Pujol, H.L. (RCA/Solid State Division, Somerville, NJ)
RELIABILITY CONSIDERATIONS FOR COS/MOS DEVICES.
Rept. No. ST-6418, 24 pp., 1975.

CMOS low power digital logic finds many applications because of its high volume manufacturing and inherent reliability. All CMOS devices are susceptible to ESD. About 50% of devices fail as a result of ESD damage, overstress or application problems. An input protection network has been devised to protect gate oxides against ESD up to 1000v. Zener diodes at the output pins can clamp the voltage to safe levels. Latchup can occur when operating above maximum ratings. Bias life tests are used to accelerate chip related mechanisms sensitive to time, temperature and voltage. Leakage mechanisms respond to bias life test. Operating life tests are switching in nature and relate to the quality of the chip process. Real time controls are accelerated tests designed by reliability and application engineers working cooperatively. CMOS devices of lower junction temperatures will provide lower failures than TTL. To detect ESD a curve tracer check is made in the area isolated by electrical test. Overstress failure is internally seen as a burned or open metallization path. Gate oxide shorts are the most common failures modes for MOS devices. They may occur in weak spots anywhere, though in a perfect MOS transistor they would occur at the four corners of the gate area. Moving ionic charges under the gate area can reduce or increase threshold voltages of ESD. Bias applied to the gate metal can cause shorts from source to drain by ionic redistribution. HTRB tests can be used to check for contamination.

13310

Gallace, L.J., Pujol, H.L., Schnable, G.L. (RCA/Solid State Division, Somerville, NJ)
CMOS RELIABILITY.
Rept. No. ST-6561, 17 pp., 1976.

This report, which presents new data on the reliability of CMOS integrated circuits, is divided into four major sections. The first section is a review of background information on MOS integrated circuit reliability, the second section presents new experimental results of comprehensive studies of the reliability of RCA CMOS (or COS/MOS) integrated circuitry, the third section is a discussion of application considerations and outlines RCA electrical specifications for COS/MOS integrated circuits, and the fourth section is a review of the effects of some of the trends occurring in the CMOS industry. Some generalizations and conclusions concerning CMOS reliability are included in the fourth section.

13319

Anon. (NASA, Langley Research Center, Hampton, VA)
ELECTROSTATIC-DISCHARGE DAMAGE TO SEMICONDUCTORS.
NASA Tech. Brief LAR-11739, 29 pp., Winter 1976.

Electrostatic discharge damage is responsible for a large number of failures in semiconductor devices. The devices examined, a J-FET, an internally-compensated op-amp and a TTL hex inverter, exhibited degradation in reverse breakdown voltage. The op-amp experienced latch-up at 80% of supply voltage. A hybrid circuit in the TTL hex inverter failed to respond to a digital command. All facilities where failures were being experienced had ESD levels in excess of those needed to produce failures. Semiconductors can be tested for ESD using a 150-200pfd capacitor and 1.5k to 2k ohm resistor model. ESD can be controlled by eliminating generators and relieving charges.

13387

Van Lint, V.A.J. (Mission Research Corp., La Jolla, CA)
MECHANISMS OF SEMICONDUCTOR JUNCTION BURNOUT.
Rept. No. MRC/SD-R-1, Contract No. DNA 001-76-C-0201, 62 pp., August 1976.

Mechanisms of semiconductor junction burnout are reviewed with particular emphasis on parameters controlling variation in energy to achieve second breakdown and device damage. Stabilizing effects promoting uniform current distribution and destabilizing effects promoting filamentary currents are identified. Those destabilizing factors involving thermal changes lead to thermal-mode second breakdown. They include resistivity peak and reverse saturation current. A nonthermal destabilizing effect at high injection conditions leads to current-mode second breakdown. The dominant mode depends on device parameters and the current level. A minimum energy needed to achieve damage can be estimated for each destabilizing mechanism from mechanisms knowledge.

13455

Porter, D.C., Price, R.D., Brooks, L.K. (Boeing Company, Seattle, WA)
EVALUATION OF PLASTIC LSI CIRCUITS.
Rept. No. D180-22945-1, Contract No. DAAH01-76-C-0455, 56 pp.

Failure analysis was performed on custom P-MOS LSI devices from field removals in a commercial telephone switching application. ESD was found to be one of the causes of failure.
ESD damage levels were investigated simulating human body RC using a 100 picofarad capacitor.

13585

Pancholy, R.K. (Rockwell International Corp., Anaheim, CA)
SOS GATE PROTECTION.
Rept. No. RADC-TR-77-134, Contract No. F19628-76-C-0192, 68 pp., April 1977.

This report describes work performed from June 1, 1976 to September 30, 1977 to investigate device design and fabrication methods for CMOS/SOS gate protection devices and circuits to be used with a radiation hardened SOS technology.

13672

Dunn, R., Ho, H.Y. (Xerox, El Segundo, CA)
INPUT PROTECTION NETWORKS ON MOS DEVICES.
Rept. No. CPT-77-6811, Components and Packaging Tech. A2-29/Ext. 1730-3303, 33 pp., December 15, 1977.

The ESD failure levels for MOS devices of various manufacturers are discussed. A failure incidence of 1% on the factory floor occurs with MOS devices having an input protection capability of 500-800v. MOS devices with protection of 1000-2000v had no failures. With multiple sources, vendors of devices with 1000-2000v are preferred. Humans are the primary source of ESD. Partially degraded networks will often continue to deteriorate and become hard failures. Overall test procedures verify the worst stress mode of charge, isolate particularly susceptible inputs and extend data base to several date codes and package types.

13717

Pancholy, R.K. (Rockwell International, Anaheim, CA)
GATE PROTECTION FOR CMOS/SOS.
IEEE - 15th Reliability Physics Symposium, Catalog No.77CH1195-7PHY, pp. 132-137, April 1977.

Pulse-power burn-out test results on SOS resistors, high voltage diodes, and thermally grown gate oxides are described. For SOS diffused resistors, the failure power per unit area ranged from 4×10^6 to 3.7×10^5 watts/cm^2 for pulse widths of 100 nanoseconds to 10 microseconds. The failure mechanism is heat-induced resistivity variation resulting in formation of low resistivity hot spots or filaments. High voltage diode and resistor combinations extended the failure voltages to 325 volts for 100 nanoseconds pulses.

13718

Minear, R.L., Dodson, G.A. (Bell Telephone Laboratories, Reading, PA)
EFFECTS OF ELECTROSTATIC DISCHARGE ON LINEAR BIPOLAR INTEGRATED CIRCUITS.
IEEE - 15th Reliability Physics Symposium, Catalog No. 77CH1195-7PHY, pp. 138-143, 1977.

Electrostatic Discharge (ESD) can easily damage bipolar integrated circuits. "Second breakdown" of NPN transistor emitter-base junctions is a common failure mode. No external emitter connection is needed for this to occur. ESD current paths, physics of ESD failure, and design concepts for improved ESD resistance are discussed.

13719

Hickernell, F.S. (Motorola, Scottsdale, AZ)
DC VOLTAGE EFFECTS ON SAW DEVICE INTERDIGITAL ELECTRONICS.
IEEE - 15th Reliability Physics Symposium, Catalog No. 77CH1195-7PHY, pp. 144-148, 1977.

The transducer electrodes of high frequency surface acoustic wave (SAW) devices can be damaged by dc voltage transients as low as 150 volts. Controlled dc pulsed voltage levels applied to SAW device aluminum interdigital electrodes on piezoelectric quartz and lithium niobate have served to define arc discharge and surface fracture conditions affecting device performance. It is recommended that high frequency SAW devices be handled as voltage sensitive parts.

13720

Gallace, L.J., Pujol, H.L. (RCA/Solid State Division, Somerville, NJ)

THE EVALUATION OF CMOS STATIC-CHARGE PROTECTION NETWORKS AND FAILURE MECHANISMS ASSOCIATED WITH OVERSTRESS CONDITIONS AS RELATED TO DEVICE LIFE.
IEEE - 15th Reliability Physics Symposium, Las Vegas, Nevada, ST-6638, 30 pp., April 1977.

All CMOS devices, which are composed of complementary insulated gate field effect transistors, IGFETS, are susceptible to damage by the discharge of electrostatic energy between any two pins. The gate oxide breakdown voltage of a CMOS device is typically 80v. Series resistors and zener diodes can clamp voltages to safe levels. Gate-oxide shorts are the most common failure mode for MOS devices. Theoretical rupture points would be located at any one or more of the four corners of the gate area. In practice, voltages may puncture a weak spot elsewhere. A circuit capacitance of 100 picofarads and series resistance of 560 ohms is used in equivalency to the human body discharge circuit. Life test showed that leakage level associated with the input protection diodes can degrade with operating life especially those prestressed to low level simulated ESD.

13757

Anon. (NASA, Lyndon B. Johnson Space Center, Houston, TX)
SAFE HANDLING PRACTICES FOR ELECTROSTATIC SENSITIVE DEVICES.
NASA Tech. Briefs, Vol. 2, No. 3, Rept. No. MSC-16642, 19 pp., Fall 1977.

The primary consideration for all electrostatic precautions is that they must be continuous. Static sensitive devices shall be identified with tags and/or labels. Personnel must follow static precautions at a static free work station including grounding of all equipment and using uninsulated metal hand tools. Plain plastic trays shall not be used for unprotected devices. Shunting clips shall not be removed until the item is in a wired circuit or receptacle. Notes on design drawings will include static warnings. DC voltages will be applied before signal voltages when testing MOS and CMOS devices. Antistatic polyethylene shall have its properties protected from degradation by immersion in water.

13974

Antinone, R.J. (BDM Corporation, Albuquerque, NM)
SPECIFICATIONS FOR MICROCIRCUIT ELECTRICAL OVERSTRESS TOLERANCE, VOL I.
Rept. No. RADC-TR-78-28, Contract No. F30602-76-C-0308, 139 pp., March 1978.

During a literature search and survey, two types of transients were identified as being important in microcircuit applications. These are electrostatic discharge transients resulting from handling and system transients generated within a system or within the environment in which it operates. It was found that the static discharge transient could be simulated by a decaying exponential pulse with a short circuit time constant of 150 nanoseconds, delivered through a source impedance of 1500 ohms. Provisions were made for varying the peak amplitude of the pulse, but a charging voltage of 1000 volts was found to provide the best screening.

Further, it was found that the system transients could be simulated by a decaying exponential pulse with a short circuit time constant of 10 microseconds, delivered from a 100 ohm source impedance. Provision was made for varying peak voltage. Different technologies require different charging levels, but a level of 50 volts was found to separate microcircuit types into sensitive and non-sensitive categories.

A pulser having the capability of delivering either the static discharge or system transient simulation pulse was fabricated. This pulser was used in subsequent procedure evaluation and sample qualification tests.

13980

Singletary, J.B., Collier, W.O., Myers, J.A. (BDM Inc., Albuquerque, NM)
SEMICONDUCTOR VULNERABILITY VOL. II.
Rept. No. AFWL-TR-73-119, Vol. II, Contract No. F29601-70-C-0019, 144 pp., July 1973.

This report presents, for a selected group of semiconductor devices, pulsed power burnout data sufficient to establish failure threshold curves. The failure curves were obtained from the experimental failure data using previously developed device failure models. This work is an extension and experimental corroboration of estimated pulse power failure levels obtained from two simple failure models which make use of device handbook parameters.

13986

Wunsch, D.C., Cline, R.L., Case, G.R. (BDM Inc., Albuquerque, NM)
SEMICONDUCTOR VULNERABILITY.
Rept. No. AFWL-TR-73-119, Vol. 1, Contract Nos. F29602-69-C-0132 and F29601-70-C-0019, 78 pp., July 1973.

This report provides an electromagnetic pulse vulnerability listing for a number of selected semiconductor diodes and transistors. The power required to cause failure was determined based on models verified experimentally. For diodes it was found experimentally that the PN junction is more vulnerable in the reverse polarity mode. For transistors testing showed the base emitter junction, in general, to be most vulnerable.

14026

Alexander, D.R., Almassy, J.B., Brown, G.L., Durgin, D.L., Jenkins, C.R., Randall, R.N., Unwin, A., Schawarz, J.J. (Boeing Co., Seattle, WA and BDM Inc., Albuquerque, NM)
ELECTROMAGNETIC SUSCEPTIBILITY OF SEMICONDUCTOR COMPONENTS.
Rept. No. AFWL-TR-74-280, Contract No. F29601-74-C-0008, 308 pp., September 1975.

This report presents the results of a program to expand and interpret the data base for EMP susceptibility of semiconductor components. The primary objective was expansion of the data base. Secondary purpose was to gain improved understanding of failure modes. Failure testing was performed on over 60 integrated circuit and 83 discrete circuit types. Specific tasks addressed were (1) IC failure modes, (2) components, (3) bulk resistance in discretes.

14075

Hickernell, F.S., Klein, R.S. (Motorola, Scottsdale, AZ)
and Ware, M.R. (U.S. Department of Defense, Fort George G. Meade, MD)
ARC GAP INPUT PROTECTION FOR CMOS/LSI CIRCUITRY.
Government Microcircuit Applications Conference, pp. 350-353, November 9-11, 1976.

Arc gaps have been used on MOS chips in conjunction with resistor, capacitor, and diode networks to provide protection against potentially damaging fast rise-time, high voltage pulses. Such pulses can occur due to equipment transients or electrostatic discharges during handling. There is little information in the literature on the operation of aluminum planar arc gap structures fabricated under standard MOS design and processing rules. A two-phase study was conducted to investigate in greater detail the use of such arc gap structures. The first phase had two objectives. The first was to identify improved arc gap structures with low ignition voltages and fast turn-on times. The second objective was to gain a better overall understanding of arc gap operation. The second phase of the study consisted of taking the glassivated arc gap structure identified as optimal in the first phase and incorporating it on a CMOS LSI logic test chip. The objective was to reduce the chip's susceptibility to damage by fast rise-time, high-voltage pulses.

14119

Ignaczak, L.R. (Lewis Research Center, Cleveland, OH)
PORTABLE SPARK-GAP ARC GENERATOR.
Nasa Tech Briefs, LEW-12886, pp. 10-11, Spring 1978.

A self contained spark-gap arc generator has been developed to simulate the electrical noise from the discharge of a static charge. The arc potentials are variable from 3 to 15kv with the energy per arc .01 to .25 joules or greater. Application has been found in testing spacecraft components. Spacecraft operating in synchronous altitudes have been surface charged to 11000 volts.

14173

Brown, W.D. (Sandia Laboratories, Albuquerque, NM)
SEMICONDUCTOR DEVICE DEGRADATION BY HIGH AMPLITUDE CURRENT PULSES.
IEEE - Transaction on Nuclear Science, Vol. NS-19, No. 6, pp. 68-75, December 1972.

If the short duration, high amplitude current pulses produced by gamma radiation in a nuclear environment flow through semiconductor devices permanent damage may result in the form of a low impedance shunt across the device junction. The current required to initiate damage in the forward direction is 5 to 15 times that necessary to initiate damage in the reverse direction. The emitter base junction is most vulnerable.

The area used to calculate power density is the active emitters sidewall area. Only a fraction of the sidewall area is involved for deep junctions. The emitter periphery plays a most important role in determining the threshold level of a device. Deeper emitter diffusions produce more tolerant devices.

Annealing of devices at 300°C for times of 1/2 to 3 hours produced significant recovery for some devices.

14284

Porter, D.C. (Boeing Co., Seattle, WA) and Bahan, M. (U.S. Army Missile Research and Development Command, Huntsville, AL)
FAILURE ANALYSIS OF PLASTIC ENCAPSULATED CUSTOM LSI CIRCUITS.
Symposium on Plastic Encapsulated/Polymer Sealed Semiconductor Devices for Army Equipment, pp. 42-53, May 10-11, 1978.

A plastic encapsulated 40 pin, 630 gate LSI PMOS circuit on a 30,000 square mil chip was introduced into commercial service in 1974. By 1977, 3.7×10^8 unit hours had been accumulated and a failure rate of 0.042%/1000 hours was demonstrated. Failure analysis was performed on 150 devices removed during the maintenance cycle with date codes spanning two years. One third were good units. Of the remaining, 55% were devices which had never worked properly and were sent to the field because they were not tested properly. Detailed autopsy efforts were completed on 70 units and no failures traceable to the packaging technique were encountered.

14646

Frankel, H.C. (U.S. Army Electronics Research and Development Command, Fort Monmouth, NJ)
THICK FILM RESISTOR ELECTROSTATIC VULNERABILITY TEST STUDY.
Rept. No. MFR-78-4, June 1978.

This report describes a Hybrid Microcircuit and Assembly Team (HM&A) investigation to develop the relative vulnerability of various thick film materials to degradation by ESD. Test specimens of alumina substrates with 31 resistors mounted were subjected to Corona, Tesla, and Polyurethane sheet tests. Measurements were made to determine the relative influence of device factors to vulnerability. Factors considered were materials, geometry, and location on substrate. Material effects were compared for observable differences to determine the most susceptible configurations.

14808

Costache, G., Goulette, D., Xavier, S. (Bell Northern Research)
ZEROING IN ON STATIC DISCHARGE.
Telesis, Vol. 5, No. 5, pp. 148-153, October 1977.

In the course of investigations over the past two years, the electromagnetic engineering department of Bell-Northern Research has reached a much better understanding of the static discharge process and how it affects equipment.

The Bell Northern research investigation explored the radiation aspect of the phenomenon in greater detail.

The electrostatic spark jumps right at the heart of the equipment and so is a sharp spike. The current and radiated field it creates, though extremely brief, can produce significant effects. They depend on the rate of change of voltage, not on the voltage directly.

Measurement probes had to be specially made to pick up the transient currents and radiated fields. As discharge current in a cabinet travels along its conducting frame it radiates energy. Other items such as cables add their own pattern. Both the electrical and magnetic components of these patterns were measured.

Radiation patterns can be contained using transient suppressing devices, shelf and rack grounding, and damage can be prevented by keeping sensitive circuit tracks away from structural or circuit members likely to carry large discharge currents.

14905

Dicken, H.K. (Integrated Circuit Engineering, Scottsdale, AZ)
INTEGRATED CIRCUIT FAILURE MODES.
Defense Microelectronics, pp. 66-68, EW/DE, October 1978.

The following are some of the stresses that will cause integrated circuit failures: radiation (alpha, beta, gamma), static electricity, vibration, power line transients, excessive hot or cold, temperature cycling, and moisture. Special conditions apply to each mode; an example is vibration. Bonding wires resonate at 30 to 50 KHz. The presence of such frequencies may cause this failure.

14960

Eichel, F.G. (Givaudan Corporation)
ELECTROSTATICS.
Chemical Engineering, pp. 153-167, March 13, 1967.

Generation of static electricity by movement of low conductivity fluids relative to each other causes the accumulation of hazardous electrical charges. This report discusses the origin and nature of electrostatic phenomena, gives methods for calculating their magnitude in practical engineering units and describes techniques for controlling and minimizing static electricity in process operations. Values for the dielectric constants, specific conductivities, and minimum ignition energies of various materials are presented.

14961

Anderson, D.C. (Richmond Division of Dixico Inc., Redlands, CA)
ELECTROSTATIC DAMAGE PREVENTION: AN OVERALL VIEW.
1978 American Defense Preparedness Association: Packaging, Handling, and Transportability Division, 17 pp., November 15, 1978.

For static protection techniques to be effective they must be applied at all times and places where electrostatic damage might occur. Simple demonstrations help to bring personnel to see the realities of static. Tape unrolled over an ash tray will pick up ashes, indicating a surface charge of 4000 volts. A neon bulb in a plastic bag will glow after being rubbed with a sweater (Anderson Effect). The point should be made that nonconductors generate charges, conductors pick them up and deliver.

14962

Kirk, W.J., Carter, L.S., Waddell, M.L. (Bendix Corp., Electronic Products Dept., Kansas City, MO)
ELIMINATE STATIC DAMAGE TO CIRCUITS.
Electronic Design, Vol. 27, No. 7, pp. 80-85, March 29, 1976.

Observed effects of ESD on JFETs included changes in the reverse breakdown voltages. The capacitance value of the discharge model influenced the voltage required to degrade the transistor. Repeated discharge pulses at voltages below the degradation level did not significantly degrade the device. Half of the JFETs showed a decrease in breakdown voltage with no significant change in the transconductance or pinch-off voltage.

Human operator-generated voltages were also measured. Peak generated voltages were observed at points where the feet of the subject partly or totally lost contact with ground plane. Conductive floors and spraying with low resistivity solvents helped to reduce environmental static.

14963

Petrick, J.T. (Naval Weapons Laboratory, Dahlegren, VA)
DISCHARGE OF AN ELECTROSTATICALLY CHARGED HUMAN.
Proceedings of the Sixth Symposium of Electroexplosive Devices, July 9-10, 1969, Franklin Institute Research Laboratories, Philadelphia, PA, 17 pp.

The results of tests outlined herein will provide valuable information that will enable valid electrostatic sensitivity tests for explosives and also aid in explaining the variation of human skin resistance with applied voltage and in determining the depth at which the charge having most effect resides. The results will also enable the analysis of possible bodily dangers involved in discharges of this nature and give considerable insight into the RF response of the human body.

14964

Amicone, R.G., Davey, C.T., Campbell, J.B. (Franklin Institute Research Laboratories, Philadelphia, PA)
ELECTROSTATIC HAZARD TO ELECTROEXPLOSIVE DEVICES FROM PERSONNEL-BORNE CHARGES.
APL-65-1, 26 pp., February 1965.

The occurrence of accidents involving electroexplosive devices (EED) has renewed interest in the static electric charge that can be accumulated and transferred by personnel. This monograph develops an electrical model to use in rough checks of EED sensitivity to personnel-borne charges: a series circuit of 500 pf capacitance and 5000 ohms resistance that can be charged to potentials up to 20 KV.

It is shown that very sensitive EED's can be fired with charges developed by personnel and it stresses caution with respect to so-called insensitive types which may be susceptible in the pin-to-case mode.

The study indicates that the hazard may be greater than anticipated and it is recommended that these limited studies be supplemented with additional investigations to furnish a firmer quantitative basis for action.

14965

Anderson, D.C. (Richmond-Division of Dixico Inc., Redlands, CA)
COMMON PLASTICS: MAJOR ENEMY OF STATIC-SENSITIVE ELECTRONICS.
Evaluation Engineering, Vol. 17, No. 2, pp. 22-24, March/April 1978.

In almost every case of electrostatic discharge damage encountered in the electronic industry, the source of the static is everyday plastic, including synthetic textiles, which are, after all, spun plastics. CMOS devices, precision resistors and countless similarly static-sensitive components are destroyed or damaged daily by this simple but misunderstood phenomenon. Even when static is recognized as the principal cause of damage, most companies fail to envision the simplicity of proper protection. They often waste money on expensive "overkill" techniques, or ignore the problem as being too expensive to correct.

14966

Anon.
HELPFUL TIPS ON COPING WITH STATIC ELECTRICITY.
Evaluation Engineering, Vol. 16, No. 4, pp. 42-43, July/August 1977.

Three devices examined illustrated ESD damage. An n-channel JFET exhibited a degradation in reverse breakdown voltage from 83v to 28v when subjected to a single discharge of 6000v. An internally compensated op-amp experienced output "latchup" to about 80 percent of supply voltage. The failure was traced to a shorted MOS compensation capacitor caused by a discharge of 1500 to 2000 volts. Finally a TTL hex inverter failed due to a beta reduction from 15 to 2. This failure was reproduced with charge of 1500 to 2000v.

14967

Anon.
COPING WITH STATIC ELECTRICITY - PART II HELPFUL IDEAS AND A DO-IT-YOURSELF SOLUTION.
Evaluation Engineering, Vol. 16, No. 5, pp. 30-31, September/October 1977.

Numerous down-to-earth tips were given including the following: conductive chairs and floors should be used as much as possible. Spray cleaning solutions have been prone to cause static. Trichloroethylene is a typical example of a cleaning solution that causes problems.

14968

Anon.
COPING WITH STATIC ELECTRICITY PART III.
Evaluation Engineering, Vol, 16, No. 6, pp. 44-47, November/December 1977.

Primary methods of coping with static electricity include using smocks made of conductive materials, controlling relative humidity, and ionized air precipitators.

Restricting personnel from wearing static charge generating clothing can result in political turmoil and regulations which would be impossible to enforce. Conductive smocks reduce such restrictions and need for enforcements.

Leakage rates for capacitive charged static voltages can be increased in a higher humidity environment; the optimum humidity range is 40-50%.

In situations where grounding and controlled relative humidity are impossible or impractical ionized air precipitators can be employed to reduce static discharge hazards.

14969

Anon.
COPING WITH STATIC ELECTRICITY - PART IV DESIGN PRECAUTIONARY MEASURES.
Evaluation Engineering, Vol. 17, No. 1, pp. 56-62, January/February 1978.

MOS input protection techniques are increasing diode size, using diodes of both polarities, adding series resistors and utilizing a distributed network effect.

Design precautions dictate avoiding crossunders beneath strips connected to external pins. Oxide thicknesses and the distances between contact edges and junctions should be carefully controlled. Transistors can be better protected by increasing the emitter perimeter adjacent to the base contact. Likewise "phantom emitters" incorporated by a second emitter diffusion shorted to the base contact add additional extrinsic base resistance ballast.

To avoid latchup in CMOS circuits, limit input current to 10 mA. For particularly sensitive CMOS devices, outputs should be isolated from cable lines via resistors and by clamping each line to V_{DD} or V_{SS} via high speed switching diodes.

In general all inputs and outside terminations must be protected via some circuit or device. All ESD sensitive items must be labeled as such and handled appropriately.

14970

Anon. (Storage Technology)
COPING WITH STATIC ELECTRICITY-PART V
STC'S NEW IC STATIC ELECTRICITY SPEC.
Evaluation Engineering, Vol. 17, No. 2, pp. 16-21, March/April 1978.

STC has initiated a wafer level oxide test that must be performed before the unit is packaged. Intel has found that testing of MOS devices with overvoltage proved more effective in eliminating potential failures than normal 125°C 168 hours burn-in. This was true, as explained, because the dominant failure mode on MOS was and still may be poor oxides.

Anti-Static Air Cap designed to cushion as well as give anti-static protection to electronic components and materials has been introduced by Sealed Air Corporation. 3M has introduced a three layer film consisting of a conductive metallic outer layer, a middle layer of polyester film and a final inner layer of heat-sealable polyethylene film.

14971

Anon.
COPING WITH STATIC ELECTRICITY-PART VI STATIC AWARENESS IS KEY TO PROTECTION.
Evaluation Engineering, Vol. 17, No. 3, pp. 45-48, May/June 1978.

The primary consideration for all electrostatic (static) precautions is that they must be continuous. Just as a precision clean part must have a maintain cleanliness requirement for all operations, a static sensitive item must have a 'maintain static free' requirement from the original component manufacturer through final production assembly.

In the vicinity of unprotected static sensitive devices avoid activities which tend to be friction producing, such as putting on or taking off smocks, wiping feet, rubbing hands, etc. Develop the habit of first touching the grounded bench top before handling static sensitive items. All equipment used at a static free work station shall be grounded, such as soldering irons and tips, lead forming tool, test fixtures and lights.

14972

Huntsman, J.R., Yenni, D.M. (3M, St Paul, MN)
COPING WITH STATIC ELECTRICITY-PART VII
A NEW TECHNOLOGY IN TRANSPARENT STATIC PROTECTIVE BAGS.
Evaluation Engineering, Vol. 17, No. 4, pp. 48-50, July/August 1978.

Because of the intrinsic deficiency in antistatic polyethylene, Static Control Systems of 3M Company has developed a new packaging material to provide transparency and the shielding effectiveness more like that of a metallic conductor. It is unique in having very low surface resistivity (less than or equal to 10^4 ohm/sqcm) but very high volume resistivity (greater than or equal to 10^{15} ohm-cm). It is a multilaminate sheet of three electrically distinct layers.

The humidity-independent conductive outer layer has a metallic coating providing a faraday cage-like protective shielding. The center layer is polyester, which provides good mechanical strength and puncture resistance. The inner layer consists of antistatic polyethylene which is heat sealable.

An ESD pulse in an antistatic polyethylene bag lasts 60-70 milliseconds and has a peak of 3000 volts. The pulse in a static shielding bag lasts just several microseconds with a peak of 75 volts.

14973

Kroeger, J., Threewitt, B. (Signetics, Sunnyvale, CA)
HEED THE LIMITATIONS OF MOS I/O CIRCUITRY.
Electronic Design, No. 6, pp. 98-105, March 15, 1974.

Because of their high d.c. impedance, MOS inputs can be damaged by static charge accumulation.

Even with protection, problems can arise with MOS circuits. Soldering with an unisolated iron, wearing silk smocks and leaving pins unterminated increase the probability of discharge damage.

A noncatastrophic failure mode occurs when input pins are left open. For example control inputs such as recirculate for a shift register, that are left open may cause a device to be in the wrong operating mode if sufficient charge is accumulated to reach the input switching threshold voltage. The device would not necessarily be damaged but would appear to malfunction.

14974

Keers, J.J. (3M Company, St. Paul, MN)
NUCLEAR STATIC ELIMINATORS - THEIR DEVELOPMENT AND USES.
Research and Development, pp. 26-29, March 1966.

The radioactive static eliminator is a self powered ionizer of air molecules. The development of 3M brand radiating microspheres presents a convenient method of safely containing the isotopes. The microsphere is a ceramic bead in which the isotope can be absorbed, then permanently sealed. The size of these beads is very small, 20-80 microns in diameter.

The use of a radioactive neutralizer for a particular application depends on a number of considerations. Cost considerations are in favor of tinsel and wire brushes if a reduction of 30000 to 10000 volts is required. If a reduction of static charge from 5000 to 500 volts is required, then a radioactive system is a must.

14975

Erickson, D.
ANTISTATIC EQUIPMENT AND TECHNIQUES.
Electronic Packaging and Production, pp. 74-96, February 1979.

Static electricity, also referred to as ESD (electrostatic discharge), has its real danger arise from the illusive "docility" of its nature. Static problems are unusual in that it is often more difficult to identify the problem than to solve it. One of the best instruments for identifying the nature of ESD damage is the SEM (scanning electron microscope).

Planning for minimizing static charges involves taking a look at all poor conductors that move. In practice there are often too many nonconductive materials involved directly or indirectly to ban all. Antistatic soldering/desoldering equipment and device carriers are available from a number of manufacturers. Conductive bags are often used for packaging protection. For the occasional requirement of antistatic coating, liquid immersion or sprays can be a practical answer. Conductive trays, containers and tote boxes help make static protection continuous. Complete static work stations are available also. Static clothing including smocks of various fiber construction and tools designed to reduce static damage are being offered in various styles. Portable work stations grounding kits complete the "arsenal".

14976

Huntsman, J.R. (3M, St. Paul, MN)
REDUCING ELECTROSTATIC DAMAGE USING PROTECTIVE MEASURES.
Electronic Packaging and Production, Vol. 18, No. 10, 3 pp., October 1978.

There is no way to totally eliminate static sensitivity; but, following common-sense anti-static procedures do a lot to protect your circuits, increase yields, improve MTBFs and lower costs. First, test all components and devices for static sensitivity. If vendors perform satisfactory testing and certification, only spot-checking is necessary. Second, specify static-shielding packaging on all static-sensitive devices coming from outside sources. Third, counsel assembly/manufacturing personnel regarding types of devices that will require special static protection. Fourth, give anti-static measures publicity; keep reminding everyone you know that static is a problem and encourage protective measures. The solution is largely one of attitudes and work habits.

14977

Kohlhaas, P. (3M Company, St. Paul, MN)
CONTROLLING POTENTIAL STATIC CHARGE PROBLEMS.
Electronic Packaging and Production, Vol. 17, No. 1, pp. 71-73, January, 1977.

While some skepticism existed one or two years ago as to whether static charge is responsible for high failure rates, it is now an accepted fact that some MOS devices can be destroyed by less than 100v of static charge.

You can ground conductive materials but you can not ground nonconductive materials. As a result anything less than a complete safeguard system is only partial protection. Clothing is not the only nonconductive material that is brought into the work station area. Items such as plain plastic tote boxes, plastic work-order sleeves or covers, candy wrappers, etc., all have the capability of blowing or degrading static sensitive electronic devices.

14978

Schreier, L.A. (Hughes Aircraft Company, Culver City, CA)
ELECTROSTATIC DAMAGE SUSCEPTIBILITY OF SEMICONDUCTOR DEVICES.
IEEE - 16th Reliability Physics Symposium, 7 pp., 1978.

Devices were chosen for ESD degradation threshold testing on the basis of high failure rates in manufacturing environments. Critical electrical parameters were measured before and after each simulated ESD. A change of more than 10 percent of the specification was considered a failure.

In addition, devices were pulsed at 75 percent of the ESD degradation threshold and then subjected to burn-in. In most cases, the critical parameter change was dramatic. Device sensitivity ranged from 100v for MOSFET to above 3KV for JFET.

The data gathered on burn-in of devices suggests that there is no long term first-order degradation mechanism if ESD levels are kept below the ESD degradation threshold.

14980

Mendelsohn, A.
TRANSIENT SUPPRESSORS
Electronic Products,Vol. 21, No. 10, pp. 31-40, March 1979.

A transient is a brief voltage pulse or surge of current that can wreck havoc in milliseconds. It may cause slow degradation, erratic operation or catastrophic failure in semiconductors, insulation dielectrics and switch and relay contacts.

Combining or "staging" of protective devices can provide overall protection unattainable with one device alone.

Silicon avalanche diode suppressors can be efficient alternatives to bulky selinium stacks used to protect SCR's triacs and diodes in solid state power control technology. Exhibiting extremely fast turn-on times these devices are available in a dozen voltage breakdown ratings between 500 and 1600 volts.

Tin, zinc, or bismuth oxide voltage dependent resistors (VDRs), often referred to as MOVs (metal oxide varistors), offer a cost effective means of dealing with high, medium, and low level transients. MOVs change resistance nonlinearly in response to applied voltage. A gradual deterioration in characteristics occurs each time a MOV conducts.

Prior to making an ultimate judgment on any given type of suppressor, a final analysis must take into account all parameters and the end product protection level desired.

14981

Williams, J.H. (General Dynamics, Pomona, CA)
COPING WITH STATIC ELECTRICITY - PART VIII ELECTROSTATIC DAMAGE TO SEMICONDUCTOR DEVICES: CAUSES AND CURES.
Evaluation Engineering, Vol. 17, No. 5, pp. 46-50, September/October 1978.

All components are static sensitive to some degree. The smaller the part, the less power it can dissipate and the more likely it is to be damaged by an electrostatic discharge.

Even now industry cannot agree on the most effective method to provide adequate protection. It frequently resorts to an expensive "overkill" practice or takes no action at all because it feels that the precautions are too expensive.

Industry experience with solid state devices has revealed numerous cases of actual or potential damage from static discharges. One of the more dramatic incidents occurred in 1964 when a polyethylene drape used as a dust cover for a Thor Delta third stage solid propelled rocket created an estimated 28000 volts as it was unrolled and accidently ignited the rocket by inducing a charge on its igniter squib.

14982

Anon.
COPING WITH STATIC ELECTRICITY - PART IX METAL FILM RESISTORS CAN BE ZAPPED BY STATIC ELECTRICITY.
Evaluation Engineering, Vol. 17, No. 6, pp. 36-38, November/December 1978.

Some evaluation engineers are not aware that precision metal film resistors are subject to damage by static electricity, and they are shocked to discover the problem.

The zapping problem occurs during sampling where some resistors are pulled out of the lot for testing. The technician walks across the room, building up a static charge on his body. Upon touching the resistor, he zaps it and it is no longer a precision film resistor with a stability of .1%. Instead, it is now a film resistor with a .2-1% tolerance.

14983

Brown, R.T. (IPL Systems, Waltham, MA)
COPING WITH STATIC ELECTRICITY - PART X.
Evaluation Engineering, Vol. 18, No. 1, pp. 54-58, January/February, 1979.

Most MOS devices contain zener diode protection to ground or substrate. Zener diodes can bleed off excess static voltages, but there is normally no protection on output pins.

To say that some ICs are not susceptible to static discharge is unrealistic, for there is a potential that can damage any chip.

The characteristic of a static charge to spread itself thin (cover all conducting surfaces) makes it a problem. The solution then is to establish a chip or board ground and ground yourself to it before work starts.

Some of the body characteristics that influence voltage levels are the dielectric constants of the clothing worn and the skin moisture level of the body.

14984

Shelton, S. (Simco Company, Lansdale, PA)
COPING WITH STATIC ELECTRICITY, PART XI, WHY USE ANTISTATIC GARMENTS?
Evaluation Engineering, Vol. 18, No. 2, pp. 28-30, March/April 1979.

Antistatic garments generally are somewhat conductive in nature and are normally worn over street clothing. In effect, they provide a type of "screen" to aid in reducing strong static fields which could induce damaging static charges on nearby electronic devices. The antistatic garment should cover all static generating clothing where possible and should at some point make contact with the person's body to provide a resistive path to ground.

A strong static field may be associated with charged clothing and radiates from it. This strong static field can induce an opposite charge on an isolated object within the field without any point or direct contact with the person's charged clothing. As long as this person remains in proximity to the object it will remain charged.

The individual being of different potential than the component causes a static discharge which may either degrade or destroy the sensitive device.

14985

Johnson, W.D. (Hughes Aircraft Company, Los Angeles, CA)
COPING WITH STATIC ELECTRICITY - PART XII STATIC AWARENESS TRAINING FOR FACTORY PERSONNEL.
Evaluation Engineering, Vol. 18, No. 3, pp. 68-72, May/June 1979.

Product reliability and production costs are directly affected by static electricity. Static controls will improve product reliability and reduce production rework or scrap. "Static Safe" ESD protection must be maintained at all times. Personnel must maintain all static free requirements for sensitive devices from the original source of manufacture through all assembly operations to point of use.

All work stations must be essentially equipped with an anti-static conductive work surface, conductive wrist band and operator ground straps, "static safe" approved label, caution signs, caution labels, static free shop carriers and approved soldering irons. Conducting materials, handling containers and packaging supplies are also necessary.

14986

Klein W.G. (United Technical Products, Westwood, MA)
STATIC ELECTRICITY: PROBLEMS AND SOLUTIONS IN COMPUTER FACILITIES.
8 pp.

Although static problems are well-recognized, their causes are not widely understood. Floor coverings (particularly carpeting) and the relative humidity are known generally to play important roles.

The matter of degree of homogeneity of conductivity is very important as most practical permanent antistatic systems involve a two-phase approach in which a small amount of discrete conductive material is added to a textile system which is otherwise nonconductive. An example of this is the introduction of conductive filaments at a predetermined spacing throughout a carpet. It has been found experimentally that conductive elements with a resistivity on the order of 10^8 ohms/cm constitute good electrostatic conductors.

One frequently hears requirements for floor coverings having static property less than 1KV or even .5KV. It is the opinion of the author that, in the absence of a specified shoe, no floor covering material can under dry conditions permanently assure performance below the 2KV level.

14987

Yenni, D.M. (3M Company, St. Paul, MN)
BASIC ELECTRICAL CONSIDERATIONS IN THE DESIGN OF A STATIC-SAFE WORK ENVIRONMENT.
Presented at Nepcon-West Conference, Anaheim, CA, 1979.

Static damage of components is fast becoming one of the most significant problems plaguing the electronics industry. Technological advances in IC manufacture such as ion implantation, ion beam milling and electron beam direct current lithography all make possible devices with higher circuit densities, higher unit performance and quite often higher static susceptibility.

Fortunately, the problems associated with static charges in the electronics environment can be controlled. To accomplish this, programs must be instigated throughout the manufacturing cycle to increase static awareness in all personnel who handle static sensitive devices. Once educated, personnel must be provided with the proper equipment to implement these techniques of static control. At the work bench this includes conductive table mats, conductive wrist straps, conductive floor mats and ionized air.

The purpose of this paper is to discuss the basic electrical requirements of the conductive components of this system in relation to the individual function each provides.

14988

Sinclair, R.E. (Lockheed Aircraft, Sunnyvale, CA)
SEMICONDUCTOR CIRCUIT FAILURE AND PROTECTION IMPLEMENTATION SCHEMES.
Nuclear EMP, Rept. No. PEM-21, 15 pp.

The transient pulse failure mechanism in semiconductor devices and thermal models for heat generation and transfer within the device are described. From these, formulas and criteria are developed to enable calculation of the critical energy for permanent damage. This is the applied pulse energy necessary for device failure. From these results, device protection criteria are developed. Protection resistor values can be calculated which permit protection of devices for specified critical energies and applied energy levels.

14989

Keller, J.K. (Lehigh University)
PROTECTION OF MOS INTEGRATED CIRCUITS FROM ELECTROSTATIC DISCHARGE.
Presented to the Graduate Committee of Lehigh University, 50 pp., 1976.

One of the primary purposes of this paper is to present a realistic model of the human body for static electric protection purposes. It is extremely important that the model be highly correlated to actual human characteristics. It is generally agreed that the best model for the human body is that of a charged capacitor, a series resistor and a relay type switch. Human body capacitance can be related to the subject's height and other physical parameters such as shoe thickness and area. Likewise human body resistance varies for different conditions (humidity, skin conditions, etc). Extensive study indicates that the human body "switch" bounces several times before making final contact. In simulated testing a high voltage relay was discovered to closely resemble the human discharge.

Protective input resistors, when fabricated from non-diffused material so that no parasitic diode results, are of little value. To be effective they must be combined with a device that will prevent the gate voltages from reaching destructive levels. Fabrication of input protection diodes must be such that the reverse breakdown voltage of the diode is less than that of the gate oxide. Thick oxide, punch through, gated punch through and field plate diodes are all designed to do this. Spark gaps are also useful precautionary devices although certain precautions with nonconducting encapsulants must be taken.

The most versatile and effective network is a gated punch through device in combination with a spark gap which may extend the protective limit to five kilovolts.

14991

Singletary, J.B., Hasdal, J.A. (BDM, Albuquerque, NM)
METHODS, DEVICES, AND CIRCUITS FOR THE EMP HARDENING OF ARMY ELECTRONICS.
Rept. No. ECOM-6085-F, Contract No. DAAB-07-70-C-0085, DA Project No. 1H6 62705 A 440, Task 01 BDM/A 24-71-TR, 55 pp., June 1971.

Electric and magnetic pulse fields generated by nuclear weapon detonations can temporarily or permanently disable military electronic equipment. Communications/electronic systems are particularly vulnerable where the pulse energy may be coupled into antennas and cables and thereby affect highly sensitive circuitry.

In the higher range of voltage applications for protective devices the use of spark gaps immediately comes to mind. Tests conducted indicate that when response occurs on a test pulse rise the response is linear. At longer pulse duration when applied voltages still exceed d.c. sparkover voltages, longer response occurs. The minimum response time for a gap may be interpreted as the sum of the times required for formulation of avalanche discharge. As a protective device a spark gap is obviously better as its response time is decreased.

Opposed series diode protection indicates this configuration is restricted in its range of passed frequencies and are susceptible themselves to EMP damage. Opposed parallel diodes offer slightly better frequency response for those applications where low voltage operation is possible. Opposed parallel diode stacks offer higher voltage protection but frequency response is lowered and response time increased.

Various diode configurations indicate usefulness in the voltage range below 90 volts, the lower limit of spark gap protection.

Supplementary analysis relates the spark gap parameter impulse ratio as defined as the ratio of surge peak voltage to static breakdown voltage. Widely observed facts indicate that higher impulse ratios produce faster response times. Analysis of the kanal equation points to the underlying factor for impulse ratios to be the ionization multiplication factor.

14992

Schade, O.H. Jr. (RCA Corporation)
ADVANCES IN BiMOS INTEGRATED CIRCUITS
RCA Review, Vol. 39, No. 2, pp. 250-277, June 1978.

The transfer characteristics of BiMOS MOSFET's throughout the nanoampere to milliampere range are presented, and their use in current mirrors, amplifiers, oscillators, and timing circuits is discussed. Linear operation in the subthreshold region is shown to provide extended performance in micropower integrated circuits, with transconductance levels similar to those of bipolar devices. Advances in MOSFET pair-matching are analyzed; commercial capabilities are described; and the combination of subpicoampere input-bias levels with protected-gate devices is shown to be practical at elevated temperatures.

14993

Hart, A.R. (Naval Electronics Laboratory Center, San Diego, CA)

PERTURBATIONS IN THE RESPONSE OF INTEGRATED CIRCUITS TO INJECTED RF POWER.
Rept. No. TN 3032, Code No. 4600, NELC R501, 32 pp., August 22, 1975.

The RF vulnerability of integrated circuits was investigated. Both interference and failure testing were performed to define the relationships between RF vulnerability and (1) fabrication technology (CMOS vs. bipolar), (2) circuit function (NAND, NOR, etc), and (3) manufacturer.

Wide variations in interference and failure power levels were found both within a device type (e.g., 5474) and between manufacturers. These variations can produce differences between one device and another by as much as 20dB for the same application. As yet, electrical screens have not been useful in predicting the vulnerability levels. It was also found that interface testing did not predict the failure power level of a device.

Based on the ICs used in the tests, CMOS devices are not susceptible to interference as bipolar (either linear or digital). But little difference exists between bipolar and CMOS for RF failure susceptibility. Bipolar linear devices appear to be the most susceptible types of devices to RF interference although some digital bipolar devices may approach these levels.

The electrical indication of interference or failure was also found to vary widely. This fact makes the diagnosis of system failures and their causes even more difficult.

14994

Kirkpatrick, C.F. (Rockwell International, Downey, CA)
PROTECTIVE REQUIREMENTS FOR ELECTROSTATIC SENSITIVE ELECTRONICS.
Rept. No. MF0004-047, Code No. 03953, 20 pp., November 19, 1979.

The primary consideration for all electrostatic precautions is that they must be continuously performed. In the vicinity of unprotected static sensitive devices avoid activities which tend to be friction producing. Before performing any work operate ionized air blowers for two or three minutes until there is no residual charge at the work area as measured by a static meter.

The antistatic precautions taken to protect individual static sensitive devices shall also be taken as applicable to protect assemblies.

Dielectric strength or insulation resistance tests are not recommended for equipment containing static sensitive devices. All unused inputs of MOS and CMOS devices must be connected to either device supply or ground. DC voltages shall always be applied before signal voltages and signal voltages shall always be removed before DC voltages.

Facilities shall include static free work stations, including metal frame work benches and conductive surfaces.

Velostat (conductive black polyolefin) is electrically conductive. Carbon particles impregnated in the poly provide volume conductivity. Sloughed particles of carbon from this material preclude its use in most precision clean operations.

14995

Anon. (RCA COS/MOS Digital Integrated Circuits)
GUIDE TO BETTER HANDLING AND OPERATION OF CMOS INTEGRATED CIRCUITS.
High Reliability Devices, pp. 6-8, 1976.

All CMOS devices are susceptible to damage by the discharge of electrostatic energy between any two pins. Their extremely high input impedance lends itself readily to the buildup of electrostatic charges.

Basic protection of these devices starts with personnel and materials all at the same or ground potential. Precautionary handling is extremely important. For example: in the sequence in which bonds are made, the V_{DD} (device supply) connection should always be made before the V_{SS} (ground) bond. Automatic handling equipment should include the use of ionized air blowers in addition to good grounding. PC boards incorporating ICs should have shorting bars installed prior to assembly.

Care must be taken in the use of input resistors as they may reduce speed because of the added RC delay.

Operation above maximum ratings can force CMOS devices into a PNPN(SCR) latch-up mechanism. "Latchup" is considered to be the creation of a low resistance path between the power supply and ground on a circuit during an electrical pulse. For latchup to occur combined beta gain is greater than 1, all junctions are forward biased, and the bias supply must supply current above holding.

14996

McAteer, O.J. (Westinghouse Corp.)
ELECTROSTATIC DAMAGE IN HYBRID ASSEMBLIES.
1978 Reliability and Maintainability Symposium, 9 pp.

Recent experience with hybrid assemblies has included ESD problems in numerous part types including bipolar devices, thin film substrates, ECL and CMOS devices. The base-emitter junction was degraded to a low resistance short and the reverse I-V curve was shifted several tenths of a volt due to the effect of ESD on several Westinghouse bipolar op-amp chips for hybrid usage. Typical damage could be induced by standing up from a lab stool and touching the package lid. Beta degradation may also occur because of ESD.

The physical mechanism of damage is aluminum transport that may thermally crack the silox overcoat in severe cases. The shorts can occur between metallization crossovers in multiple layer metallizations. A quasi-square anomaly often is detected by SEM after static discharge.

This square pattern was observed in simulated ESD testing.

ESD failures were observed to cause several tenths of a volt shift in the emitter outputs of ECL devices. Damaged oxide over the E-B junction could be seen near one end of each emitter contact area. Multiple damage to ECL from ESD resulted in several cases of shorts between V_{CC} and ECL outputs, also in leaky reverse base-emitter junctions.

The cholesteric liquid crystal method was used to detect the exact short site caused by ESD in several CMOS devices. Subsequent testing under various loads found CMOS devices least susceptible with nothing attached to any nodes rather than having one or more nodes grounded.

14997

Wetherald, M. (Tektronix Manufacturing)
SPECIAL HANDLING OF STATIC SENSITIVE DEVICES.
Tektronix Interoffice Communication, 12 pp., June 17, 1975.

Component evaluation and manufacturing engineering groups have been involved in some experiments to determine the magnitude of the static problems with semiconductors in Tek Manufacturing. Several electronic devices were subjected to typical production handling, then tested. Out of 50 MOS devices tested, five had parameters degraded and five more were catastrophic failures. Techniques to minimize handling and the use of conductive containers such as Velostat can reduce losses in manufacturing. Multimeters and other testing devices must also be used with care on MOS IC's.

14998

Olin, R.P. (Control Data Corp.)
"CONDUCTILE" STATIC CONDUCTIVE VINYL FLOORING.
Rept. No. HPOC-79029-EMO1, Charge No. 54kkM94, March 30, 1979.

The "conductile" test sample submitted by Vinyl Plastic Inc. (VPI), Sheboygan, Wisconsin passed the current CDC requirement for maximum generation of static electricity in a computer room environment.

The test conducted by Control Data Corp. measured the voltages generated when a tester generated standard voltages by shuffling his feet on a test carpet using neolite soles.

No measured voltage was generated when a test sample tile was cemented to a metal 2'x2' floor with conductive cement.

14999

Johnson, W.D., Weekley, R.R. (Hughes Aircraft Company, Los Angeles, CA)
MELAMINE LAMINATE AND RCAS-1200 WORK SURFACE MATERIALS, EVALUATION STUDY.
Rept. No. IDC 7611.34/76, 11 pp., January 16, 1978.

An evaluation was conducted on two work surface materials to determine if they are acceptable as static safe.

The test results indicate that melamine laminate is an acceptable "static safe" work surface. The antistatic properties of melamine laminate are unaffected by exposure to low relative humidity and to various cleaning agents.

The antistatic properties of RCAS-1200 "pink poly" are not degraded by low humidity but are seriously degraded by all cleaning agents except antistatic fabric softeners such as "Downy".

15000

Warsher, A. (Charles Stark Draper Laboratory, Cambridge, MA)
USE OF MELAMINE WORK SURFACES FOR ESD POTENTIAL BLEED-OFF.
Rept. No. PG-H-242-78, 11 pp., September 22, 1978.

Paper-base melamine sheets can be used for work surface tops under certain conditions. The conditions are as follows: the top surface of the melamine be abraded away before applying a spring loaded contact for electrical ground, the ambient relative humidity be above 30% if the work surface will be relied upon for electrical discharge, the earth return circuit not be through an additional current limiting resistor, and other ESD measures be continued such as the use of operator wrist straps.

Metal bench tops using a 250,000 ohm resistor to ground are still the preferred method for ESD protection of work stations.

15001

Madzy, T.M. (IBM Corp, Endicott, NY)
FET CIRCUIT DESTRUCTION CAUSED BY ELECTROSTATIC DISCHARGE.
IEEE - Transactions on Electron Devices, Vol. 23, No. 9, pp. 1099-1103, September 1976.

MOSFETs are particularly susceptible to ESD damage because of the low destructive breakdown voltages of their oxides.

In IC FET packages the PD is normally another FET with its gate and source connected to the substrate and is in effect a voltage limiting diode with the result that ESD potentials are developed directly across its gate oxide. The I-V curve of the device can depend on whether or not a potential exists at the ground pin of the module.

The destruction of the gate oxide is due to joule heat and arc action when the potential across the device is 5-10 MV/cm. ESD pulses less than 12ns in width require large magnitudes to cause destruction. Pulses of greater than 130ns width require magnitudes of 44v.

The lowest ESD susceptibility level occurs when the substrate is connected to an electrostatic source through some very low impedance return and a charged human makes contact with one module pin.

15002

Enoch, A.F. (Sanders Associates, Inc. Nashua, NH)
ELECTROSTATIC DISCHARGE DAMAGE PREVENTION.
Sanders Associates Federal Systems Group, Rept. No. 815032, Standard No. 228, FSCM94117, 5 pp., August 31, 1976.

Sanders Associates, Inc. have established Corporate Standard SA-STD-228 for Electrostatic Discharge Damage Prevention. Corporate Standard 228 includes provisions for distribution of ESD sensitive device listings, purchase specification preparation, engineering drawing and parts list callouts, assembly markings and maintenance manual cautionary notes.

Employee training and basic awareness requirements are specified and the use of protective antistatic devices is required.

15003

Koenigsberg, H.M. (Hughes Aircraft Company, Los Angeles, CA)
ANTI-STATIC PROTECTION FOR THE PCB YELLOW ROOM AREA.
Rept. No. 4500-585, 5 pp., March 3, 1978.

The most practical method of minimizing or eliminating the effects of static electricity is by ionization using the high voltage discharge of alternating current. The contamination problem in the yellow room of PCB manufacturing is aggravated by the use of processing materials, paper articles and work in progress. Laminar flow hoods can effectively eliminate 2-3kv charges at 3½' distance within 5 seconds. Several sequential processing steps must be carried on and several different materials utilized before the net effect on product yield can be determined.

15005

Gardner, P.R. (TRW, Redondo Beach, CA)
HARDNESS ASSURANCE LATCHUP SCREEN PROCEDURE.
Defense Nuclear Agency, Rept. No. 31442-6001-RU-00, Code No. B323077464, Z99QAXTD072-07, M2590D, 23 pp., November 23, 1977.

There are two types of radiation induced latchups, a hard latchup and an incipient latchup. A hard latchup is a sustained functional failure. Incipient latchup is not sustained but lasts longer than can be explained by normal circuit times constants.

The source used to promulgate radiation induced latchup will be a flash X-ray machine or a Linac. A dry run radiation exposure and a pass status to verify dosimetry will be performed.

Oscilloscopes or pre-set comparators will monitor outputs to verify device parameters.

The method to analyze four layer integrated circuit latchup is valid for bipolar junction-isolated and dielectrically isolated integrated circuits.

The latchup or PNPN sustaining mechanism in a bipolar integrated circuit occurs in four-layer bistable structures. One operating state is characterized by high impedance, low current while the second state is characterized by low impedance and high current.

The existence of a PNPN structure within an integrated circuit does not imply that it is a sustainable latchup path even if the parameters for bistable action are present. For a latchup to be sustained, a bias of positive polarity from anode to cathode must be present; in addition, the current must not be limited below holding. For example, if an intermediate function is reverse-biased latchup is not possible.

15006

Anon. (Vinyl Plastics Inc, Sheboygan, WI)
INSTRUCTIONS FOR INSTALLATION AND MAINTENANCE OF CONDUCTILE.
MK-20150175 Patterns: (CON2, CON3, CON4, CON6, CON8, CON18), 7 pp.

Static conductive vinyl flooring must be installed on smooth, dry, clean, subfloors. New concrete must be properly cured preferably by covering it with polyethylene film. Under ideal conditions a drying time of at least eight weeks is required.

Conductive flooring will not be guaranteed if the rate of moisture emission from subfloor exceeds three pounds per 1000 sq ft per 24 hours. Conductile may be installed on radiant heated floors provided the surface temperature does not exceed 90°F.

Installation of conductile directly over wood strip or plank subfloors is not recommended.

15007

Hermansen, D.D (TRW, Redondo Beach, CA)
PACKAGING SPECIFICATION ELECTRONIC COMPONENTS, SMALL, PACKAGING OF.
Rept. No. PK4-22B, 19 pp., June 13, 1975.

This specification covers the preservation, packaging, field force protection, and container marking of all types and versions of established reliability small electronic components.

Components that are electrostatic sensitive as defined in M283308 or as determined by manufacturer/supplier shall be handled as specified in M283308 and protected as specified in 3.1.5.2. Electromagnetic, magnetic or radioactive field force protective metals shall not be in direct contact with the component.

Electrostatic protection shall be provided by a shorting of leads or by electrostatic shielding provided by the packaging method utilized.

Electromagnetic protection shall be provided by overwrappping the component already packaged as required for ESD with aluminum foil conforming to MIL-A-148.

Radioactive protection shall be accomplished through the use of lead-filled compositions completely encasing the component.

15008

Mirakentz, A. (TRW, Redondo Beach, CA)
INSTALLATION AND OPERATION OF STATIC-FREE WORK STATIONS.
Rept. No. 027, 5 pp., October 1, 1975.

The purpose of this manufacturing alert is to provide Manufacturing and Product Assurance personnel with general information for the installation and operation of static-free work stations and for the proper handling of static sensitive devices.

The preferred work station is the standard metal-framed Line Master bench. The work surface must be covered with either a metal plate or an antistatic polyethylene sheet. It is recommended that metal plates be used primarily on bench tops where high heat generating equipment such as solder pots are used. In all cases both the antistat and metal bench must be grounded.

All tools and equipment used at the station must be grounded. Plastic lead forming tools shall not be used.

In special cases where grounding of the operator to the work station is impractical an air ionizer/blower must be used.

There are no special storage requirements for static sensitive devices provided they are properly packaged.

15009

Dawe, W.E. (TRW, Redondo Beach, CA)
ELECTROSTATIC (STATIC) SENSITIVE PARTS, LISTINGS, IDENTIFICATION, MARKING, HANDLING, AND PACKAGING OF.
Rept. No. M283308, Code Ident. No. 11982, 13 pp., July 21, 1975.

This document provides a list of components currently being procured at TRW that are considered electrostatic (static) sensitive. Also included are guidelines for handling and packaging.

Test fixtures shall be equipped with a short across the terminals which is disconnected after the device is inserted.

All low-impedance signal generators or power supplies should be disconnected or the power source output should be slowly reduced to zero before disconnecting from the device.

After burn-in, maintain electric bias until the device has cooled to room temperature. Cotton gloves shall be used during loading and unloading of burn-in racks.

15011

Sixel, D.E., Gaspard, K.R. (Honeywell, Defense Systems Division)
HANDLING OF ELECTROSTATIC SENSITIVE ELECTRONIC ITEMS.
Rept. No. ES8708, Code No. 08638, 27 pp., April 5, 1976.

Category 1 components of ESD senstive parts are very sensitive to ESD induced degradation having the worst case sensitivity range of 0 to 170 volts. Category 1 assemblies are any assembly containing a Category 1 component. Category 2 components worst case voltage sensitivity is 171 to 2000 volts; Category 3 is 2001 to 15000 volts; Category 4 is 15000 volts.

All personnel involved in the handling of ESDS categories 1, 2 and 3 devices shall receive instructions and proper training in the implementation of the control measure requirements and guidelines specified herein. To be certified, all personnel shall attend and successfully complete a formal training program.

ESD sensitive parts shall be transported to and from the stockroom area in the "as received" package when the package has not been damaged. Do not open individually packaged parts for count or issuance (kitting). Personnel shall not unnecessarily handle any device received which indicates it is an "ESDS" device.

15012

Meul, J. (Raytheon Company)
ELECTROSTATIC SENSITIVE DEVICES, MARKING AND HANDLING THEREOF.
GIDEP Rept. No. 347.23.00.00-K9-02, Access No. E024-1176, GIDEP Originators Rept. No. 1-GEN-00075, 16 pp., August 20, 1974.

Prior to removing static sensitive devices from their protective packages the following pre-test conditions should exist: provide 40% (minimum) relative humidity at the test station; line all trays or boxes for carrying device with ¼ thickness conductive cushioning; avoid touching leads or contacts even though grounded; avoid unnecessary physical activities which tend to be friction producing. The original package should be in contact with the conductive surface of test station when being opened or closed. Foil wrapped devices may be placed in any type of container.

15013

Troeger, E.P. (Aerospace Industries Association of America, Inc. Washington, DC)
REPORT ON MC-118, STATIC SENSITIVE PARTS AND EQUIPMENT PROTECTION.
Report No. AO-MC 73-86, 20 pp., December 4, 1973.

Surveys showed industry was facing potential ESD damage to components and had serious problems throughout the manufacturing assembly and shipping activities.

Semiconductors, chips and other component parts are generally sensitive until fabricated or installed in assembly. To eliminate this possibility, the receiving inspection of electronic items should be moved to a controlled area and "good practice" suitable for handling static sensitive classes of parts should be initiated. The above findings showed a general lack of understanding of field force protection and the basic electrical phenomena involved.

15014

Tasca, D.M. (General Electric Company, Space Division, Philadelphia, PA)
PULSE POWER FAILURE MODES IN SEMICONDUCTORS.
IEEE - Transactions on Nuclear Science, Vol. NS-17, No. 6, pp. 364-372, December 1970.

It was observed that a common mode associated with permanent damage effects in reverse-biased junctions is the phenomenon known as "second breakdown." Both energy and current modes were observed.

The occurrence of thermal second breakdown which is energy-dependent was found to represent the point of incipient permanent damage at submicrosecond pulse conditions. In contrast the energy required for current mode second breakdown has not in itself been observed to represent incipient junction damage. Thermal second breakdown physically is a local thermal runaway effect at the junction induced by severe current concentration. Current mode second breakdown has not been fully understood or observed. It is initiated by relatively high material current densities under the emitter during collector to base junction reverse pulsing resulting in a forward bias on a portion of the emitter.

Comparison of the mathematical model with experimental data indicates that if the volume of the thermal second breakdown current constriction site across the junction and the critical initiation temperature are known then the model can be used to determine the pulsed power susceptibility of any general P-N junction. On a practical basis it is relatively easy to assign specific values to the initiation temperature and to empirically determine the typical current constriction site volumes.

15015

Gallace, L.J. Whelan, C.D. (RCA)
ACCELERATED TESTING OF COS/MOS INTEGRATED CIRCUITS.
RCA Solid State Technical Reprint ST-6379, pp. 2-4.

The predominant pitfall of accelerated-stress life testing of COS/MOS integrated circuits is that the failure mechanism may change as the stress level is increased. Interactional problems where more than one stress is changed at the same time may also cause the major degradational process to change.

There is no way to accelerate a "random" failure because by definition there is no predictable pattern of causing such failures. It is important to remember that in accelerated testing the probability of failure is a function of stress and time. The objective of accelerated testing is the production of an acceleration curve which relates applied stress and time for a particular level of failures.

The constant stress level of accelerated testing involves the development of a distribution of failures with time. The step stress level involves failure distribution at a definite stress level and time intervals.

With the use of Arrhenius equation and a plot of temperature accelerated life-stress testing a quantitative relationship between temperature and time can be developed. The activation energy of the failure mechanism must, however, be known.

15016

Lee, J. (Raytheon, Portsmouth, RI)
93L415 BOARD FAILURES.
Rept. No. 7380, Raytheon Part No. 907715-103, E075-0071, 3 pp., May 10, 1977.

The failure mechanism causing the input leakages of the 93L415 to increase was due to electrical overloading of the input protection diode caused by static discharge. The devices that failed were six 93L415s in ceramic packages. All six units exhibited at least one input pin which exceeded the high input current parameter specified at 40ua at V_{IN} = 4.5v and V_{CC} = 5.25v.

15017

Patterson, J. (Teledyne Microelectronics, Manager Failure Analysis Laboratory)
A TEST METHOD TO DETECT ELECTROSTATIC DAMAGE IN THICK FILM RESISTORS.
IEEE - 78 Advanced Techniques in Failure Analysis Symposium, pp. 35-38, 1978.

The test method described herein allows the examinations of high voltage characteristics of thick film resistors and reveals the voltages to which they have previously exposed. The model that best fits recorded data to explain why thick film resistors decrease in value when subjected to ESD is thin oxides surrounding resistive particles in thick film ink. During exposure to high electric fields these oxides break down permanently and provide additional conduction paths within resistors.

15018

Anon. (Naval Sea Systems Command)
MILITARY SPECIFICATIONS, STANDARDS AND CONTRACT CLAUSES SPECIFYING CONTROLS FOR PROTECTION AGAINST ELECTROSTATIC DISCHARGE.
NAVSEA S6000-AB-GTP-010, 51 pp., December 1978.

Excerpts of military documents regarding ESD controls are contained herein. Military documents MIL-E-16400G, MIL-STD-454E, MIL-M-38510, MIL-S-19500, and MIL-I-983E cover design specification requirements. Military documents MIL-S-19491E, MIL-M-55565A, MIL-STD-1475, MS90363, NAS853 and various NAVSEC contract clauses delineate packaging specifications. Technical manuals MIL-M-15071G, MIL-M-24100, MIL-M-21742A, MIL-STD-1604 and MIL-M-7298C contain overhaul and maintenance procedures for protection against ESD. MIL-STD-100A and MIL-D-1000A are drawing specification requirements for ESD items.

15019

Stadler, P.H. (Philco-Ford Corp., Aeronutronic Division, Newport Beach, CA, and Harry Diamond Laboratories, AMXDO-EM, Washington, DC)
FAILURE THRESHOLD AND RESISTANCE OF THE PROTECTED AND UNPROTECTED 2N2222 TRANSISTOR IN THE SHORT PULSE WIDTH REGIME.
Nuclear EMP, PEM-7, Contract No. DAAK02-70-C-0464, 48 pp., May 1972.

This work was authorized under MERDC, Ft. Belvior, contract No. DAAK02-70-C-0464 funded by the Defense Nuclear Agency. The effort included the design, construction and checkout of a fast, high voltage pulser with a component test effort. This latter work is emphasized in this report; the operator's manual covers the details of the pulser.

15020

Hart, A.R. (Naval Electronics Laboratory Center, Electron Material Sciences Division, San Diego, CA)
RF FAILURE PREDICTION FOR MOS 4001 AND 4011 INTEGRATED CIRCUITS.
Rept. No. NELC R501, Code No. 4600, TN3107, 47 pp., January 19, 1976.

This report defines the effects of a single, high-power, 5 microsecond, 3 GHz RF pulse injected into the output of two types of MOS devices: 4001 (NOR Gate) and 4011 (NAND Gate). This report presents a possible theory which explains the 12dB difference in power level for RF failure of the devices tested and compares the effects of different manufacturers' chip layout designs on the RF susceptibility of these devices. A DC model was developed and applied to the RF problem and found to fit very well to the experimental data. The DC model predicted the RF susceptibility hierarchy for several manufacturers and helped to define potential ways of reducing the RF susceptibility of these types of MOS devices. This report also points out how some EMP radiation hardness protection circuits may actually increase the RF susceptibility of similar types of devices.

15022

Huntsman, J.R., Yenni, D.M. (3M Company, St. Paul, MN)
DON'T ZAP IT - BAG IT.
Quality, pp. 18-21, December 1978.

Advances in IC technology are increasing circuit densities and thus accentuating static damage susceptibility. Protective devices are not always a guarantee of protection. Insulators have a very large surface resistivity and therefore do not dissipate static electricity. Organic additives can increase their conductivity on their surfaces. Antistatic bags do not effectively protect their contents from external electric fields. Charges may accumulate, forming a significant voltage gradient from top to bottom. 3M Company has developed an effective field shielding antistatic bag consisting of an outer metallic coating, a center polyester film, and an inner antistatic polyethylene. The ESD pulse in this shielding bag lasts only several microseconds with a peak of 75v.

15023

Ramaley, J.W. (3M Company, St. Paul, MN)
VELOSTAT VS ANTI-STATIC FILMS.
15 pp., May 12, 1975.

Antistatic film surface resistivity tests show that it falls into the range of an insulator. Velostat is 100 million times more conductive than anti-static films. A test was run at 35% RH. A subject with static charge of 1000v touched a grounding strap of velostat conductive plastic. The voltage dropped to 0 volts instantaneously. The decay time was less than 1/10 second regardless of humidity or electrode. Age affects the anti-static qualities of certain anti-static films.

Electric ionizing air blowers induce low but significant voltages in ungrounded objects brought near it; nuclear powered blowers do not.

15024

Oishi, T. (Naval Sea Systems Command, Washington, DC)
ELECTROSTATIC DISCHARGE IMPACT ON ELECTRICAL/ELECTRONIC DEVICES, COMPONENTS, ASSEMBLIES AND EQUIPMENT.
Association of Scientists and Engineers 16th Annual Technical Symposium, 1979.

The hazard of ESD is an existing problem which is becoming more severe with the advancement of technology. Government and Navy personnel lack knowledge on the hazard of ESD. This lack of knowledge is resulting in unnecessary repair costs, excessive equipment downtime and reduced mission effectiveness in that electrical/electronic devices and equipment which incorporate them are being damaged throughout the equipment life-cycle during processing, assembly, inspection, packaging, shipping, storage, testing and maintenance.

An awareness program on ESD along with the implementation of an effective ESD control program can minimize the ESD hazard.

15025

Krulac, I.L. (IITRI/RAC, Griffiss AFB, NY)
AUTOMATED MACHINE PRECAUTIONS FOR MOS/CMOS.
Rept. No. RAC-74-01PM, 3 pp.

A retrospective search/survey was performed to determine precautions necessary in handling MOS or CMOS devices in automatic test and insertion equipment. The problem that exists in handling these devices is the build-up of large amounts of static voltages on portions of machine handling equipment. The static charge build-up is approximately 10,000 volts depending on humidity levels.

15026

Branberg, G. (Hewlett-Packard, Interoffice Correspondence)
L.I.D. ELECTRO-STATIC DISCHARGE STUDY. Rept. I, Rept. II, Rept. III and Rept. IV.
February 1978, April, 1978, May 1978, June 1978, respectively.

An electrostatic discharge (ESD) study was performed in order to provide the R&D engineer with data necessary to properly protect sensitive components from ESD damage and the production and service engineers with information necessary to determine appropriate antistatic production assembly and repair techniques.

The study consisted of an ESD susceptibility comparison on CMOS devices from various vendors. A latent failure life test was also performed.

A test station was assembled capable of delivering a repeatable discharge to the D.U.T. and a standard test method was developed for determining ESD sensitivities for this study.

15027

Kenworthy, C. (John Fluke MFC. Co., Inc.,)
STATIC-SENSITIVE DEVICE FAILURES, A CONTROLLED EXPERIMENT.
7 pp., January 14, 1977.

It is very apparent that the overall failure rate caused by static discharge can be reduced dramatically for both CMOS and low-power Schottky by careful handling. Opto-isolaters can benefit from delicate handling. The failure rate for CMOS was cut 88% and 76% for low-power Schottky by the application of the recommended handling procedures.

15028

Polski, P.A. (Sperry/Univac)
ELECTROSTATIC DISCHARGE STUDY REPORT.
Rept. No. 12561, UD1-3792-2, 15 pp., March 30, 1978.

This study was initiated to determine what parts used by Sperry Univac Defense Systems Division are potentially sensitive to electrostatic discharge. Device structural features influence ESD susceptibility. Components very sensitive to ESD damage (Cat. I) include MOS with no input protection circuitry, dielectrically isolated semiconductors with internal capacitor contacts connected to external pins and microcircuits utilizing N+ guard ring construction (with metallization crossing over the guard ring). Category II devices include MOS with input protection, dielectrically isolated and fine metal bipolar, low power Schottky and Schottky TTL, high speed ECL, high input impedance linear (greater than or equal to 10^7 ohms) junction FET's, small signal transistors with f_T greater than 500 MHz, and all devices that use metallization paths over active areas and ladder networks.

15030

Anderson, D.C. (Richmond-Division of Dixico Corp., Redlands, CA)
MILITARY RECOGNIZES NEED FOR ELECTROSTATIC DAMAGE PREVENTION IN ELECTRONIC DEVICES, COMPONENTS, ASSEMBLIES AND EQUIPMENT.
1979 Spring Symposium - American Defense Preparedness Association: Packaging, Handling, and Transportability Division, 4 pp., April 25-26, 1979.

Efforts to help standardize and increase awareness of the ESD protection problem are underway. Military Standard, MIL-STD-xxx entitled "Electrostatic Discharge Control Program for Electrical and Electronic Devices, Components, Assemblies and Equipment," and Military Handbook, MIL-HDBK-xxx entitled "Electrostatic Discharge Control Handbook for Electrical and Electronic Devices, Components, Assemblies and Equipment," were prepared under Mr. Toshio Oishi. Mr. Oishi is now Systems Effectiveness Branch Head, Naval Sea Systems Command, Combat Systems Directorate, Washington, D.C. 20362 (Code 61C) Phone 202/692-6426.

15046

Anon. (Naval Surface Weapons Center, White Oak, MD)
ELECTRO-MAGNETIC PULSE RADIATION ENVIRONMENT SIMULATOR FOR SHIPS.
Rept. No. NSWC MP 79-37, 16 pp., 1979.

EMPRESS is a facility of the U.S. Navy to test ship behavior in a simulated EMP environment. This brochure presents what EMPRESS is, why it is needed, and how it is used.

15056

Sonenclar, R.J.
EIA SEES CODE OVERKILL - ELECTROSTATIC SAFE-GUARDS.
Electronic Buyer's News, Issue 202, June 18, 1979.

The EIA has criticized the Government's effort to institute more rigid safeguards for the control of electrostatic discharge. Industry officials assert that only one half to three quarters of the users' industry has taken adequate steps to combat the problem. The Navy is seeking to develop a standard which would mandate compliance before companies using ESD sensitive devices would be approved for government contracts. The EIA cites cost factors and an "overkill" mentality as causing unreasonably high cost impact.

15057

Pease, R.L. Alexander, D.R., Jenkins, C.R. (BDM Corp., Albuquerque International, Albuquerque, NM)
ELECTRICAL OVERSTRESS TEST PROGRAM AND INTEGRATED CIRCUIT FAILURE MODE EVALUATION.
Rept. No. DNA 4467F, Contract No. DNA 001-77-C-0156, Subtask 299QAXTB097-04, 108 pp., April 26, 1978.

This final report describes the SOS diode test structures which will be used for empirical investigation of electrical overstress failure. The test structures, in which important physical parameters are varied, are described in detail and a test plan is presented for the overstress testing that will generate failure data for a sensitivity analysis of pulse power failure level as a function of junction area, epitaxial thickness, junction radius of curvature, doping level and metallization and diffusion spikes. An electrical overstress failure mode and distribution study in integrated circuits is presented. Data on over 1200 devices which were tested on previous programs were analyzed to determine failure modes on DTL, RTL, TTL, ECL, MOS and linear integrated circuits. The failure distributions on over 3,000 devices from several different test programs were reviewed to identify "mavericks." These "mavericks" were investigated for distinctive failure modes or unusual preirradiation electrical characteristics.

15058

Anon.
NAVSEA ZAPS ESD.
Overview, pp. 17-21, Spring 1979.

The Naval Sea Systems Command is preparing a new MIL-STD and a new MIL-HDBK to educate personnel as a primary deterrent to ESD damage. The Naval Material Command has asked NAVSEA to formulate an instruction on ESD damage prevention procedures also.

The Naval Supply Systems Command (NAVSUP) has instituted contract-required procedures for manufacturers to insure proper packaging of ESD sensitive devices. NSN's have been assigned to commercially available antistatic packaging materials.

The NEARTIP components analyzed by Honeywell have caused the establishment of facility-wide ESD control systems.

15059

Huang, C.L., Kwan, F., Wang, S.Y., Galle, P., Barrera, J.S. (Hewlett-Packard Co., San Jose, CA)
RELIABILITY ASPECTS OF 0.5um AND 1.0um GATE LOW NOISE GaAs FETS.
IEEE - 17th Reliability Physics Symposium, pp. 143-149, 1979.

GaAs FET failures are obviously catastrophic events. Long-term events such as changes in Schottky gate characteristics and intermetallic reactions can eventually cause loss of gate control. Specifically an explanation and solution to the potential reliability problem of electrostatic discharge-created changes in Schottky gate reverse leakage currents.

The changes vary in degree from just discernable creation of a resistive reverse current to catastrophic eruption of gate metal, GaAs channel and source contact metal.

15060

Anon. (Naval Sea Systems Command, Naval Electronic Systems Command)
ELECTROSTATIC DISCHARGE (ESD) DAMAGES INTEGRATED CIRCUITS AND DISCRETE SEMICONDUCTOR DEVICES.
Electronics Information Bulletin, NAVSEA 0967-LP-001-3975, 8 pp., May 15, 1978.

The purpose of this article is to provide an awareness of (1) common sources of static, (2) detrimental effects, and (3) available controls for protection from the damaging effects of electrostatic discharge (ESD). Particularly susceptible to damage from ESD are metal oxide semiconductors, discrete bipolar transistors and diodes. Damage does not always result in sudden failure but may produce degradation, often apparent as reduced reverse voltage breakdown.

15074

McAteer, O.J.
SHOCKING BLOW TO MILITARY ELECTRONICS.
Military Electronics/Countermeasures, pp. 59-63, June 1979.

ESD has been recognized in recent years as a major source of electronic device failures. The problem becomes even more acute for military applications where reliability is a critical parameter and semiconductor part counts are high. Subtleties in physical analysis make recognition of ESD failures difficult. More thorough analysis such as chemically etching the SiO_2 passivation layer and site isolation using special heat sensing cholesteric crystals are used. Capacitive coupling and loading between nodes is another subtlety making ESD failure analysis even more difficult.

15083

Woods, M.H., Gear, G. (Intel Corp., Santa Clara, CA)

A NEW ELECTROSTATIC DISCHARGE FAILURE MODE.
IEEE Transactions on Electron Devices, Vol. ED-26, No. 1, pp. 16-21, January 1979; 16th Reliability Physics Symposium, pp. 146-150, 1978.

A new electrostatic discharge failure mode was discovered which affects MOS LSI components in hermetic packages with nonconductive lids. Failure can be induced by spraying package lids with canned coolant. It is shown that charge from the freeze spray causes breakdown in the air-gap between the die surface and the lid. As a result, localized surface charging and field inversion occurs in the array, which produces leakage currents and circuit failure. The failure mode can be characterized by its recovery with either a strong UV exposure to the die surface or a DI water rinse.

15084

Griffith, O.K., Bequwala, M.M.E., Johnson, R.E. (Rockwell International, Autonetics Group, Anaheim, CA)
NONDESTRUCTIVE SEM STUDIES OF LOCALIZED DEFECTS IN GATE DIELECTRIC FILMS OF MOS DEVICES.
IEEE - 14th Reliability Physics Symposium, Rept. No. X76-554/501, 4 pp., April 20, 1976.

A nondestructive technique to identify localized defects in the gate dielectric of MOS devices has been developed. The technique is based upon electron beam induced conductivity modulation which gives rise to a relatively large increase in gate current under an applied bias when the beam scans a localized defect area. Measurements on devices with low gate breakdown voltage have been made and correlated with regions where subsequent catastrophic gate breakdown occurred. A circuit description and physical model of the technique is presented.

15085

Tasca, D.M. (Boeing Aerospace Company, Seattle, WA)
PULSE POWER DAMAGE CHARACTERISTICS OF ELECTRICAL RESISTORS.
Vol. 1, Rept. No. AFWL-TR-75-108, Contract No. F29601-74-C-0008, D224-13058-1; TD-4-23, 90 pp., April 1976.

This report defines the EMP induced damage characteristics of a variety of electrical resistor types. The experiments evaluate the change in device resistance. Of the five resistor classes tested, wire wound resistors were most resistant followed by carbon composition, carbon film, metal film and metal oxide, respectively.

15086

Grimm, A.V. (Bendix, Kansas City Division)
LSI INTEGRATED CIRCUIT TEST DEVELOPMENT.
Rept. No. BDX-613-1017, Contract No. AT(29-1) 613 USAEC, 62 pp., March 1974.

Methods for handling and testing MOS semiconductor IC's used in the prevention of overstressing by ESD were investigated and developed. Testing was performed in six areas of static discharge damage: DC testing, process evaluation test circuits, DC testing of MOS LSI devices, functional testing of MOS devices, switching time testing of MOS devices and fault testing of MOS devices. The Fairchild 5000 C with low frequency generation was capable of only limited testing of the MOS LSI devices.

15087

Anon. (Hewlett-Packard Co., Palo Alto, CA)
LAB MANUAL ENVIRONMENTAL EVALUATION AND QUALIFICATION TESTING.
55 pp., May 1975.

This manual provides HP Data Systems Division with a single document covering many of the considerations associated with developing, testing (including a test for ESD susceptibility) and specifying the environmental capabilities of Data Systems Products.

15088

Leopold, H.S., Rosenthal, L.A., Laib, G.R. (Naval Surface Weapons Center)
INVESTIGATION OF TECHNIQUES TO REDUCE ELECTROSTATIC DISCHARGE SUSCEPTIBILITY OF EED'S CONTAINING PLASTIC PLUGS.
Rept. No. NSWC/WOL/TR 78-82, 31 pp., August 25, 1978.

The substitution of a conductive plastic for the normal dielectric plastic was considered the most satisfactory retrofit to provide human electrostatic discharge protection for electroexplosive devices (EED's) employing plastic plugs. Conductive gaskets may also be satisfactorily used for protection in those cases where the length of the EED can be increased.

15091

DiCiaccio, C. (GTE Sylvania)
40 PIN PMOS INTEGRATED CIRCUIT.
Rept. No. E0176, Project No. 479-5735, pp. 2-8, May 26, 1976.

Three PMOS devices were subjected to increasing stress levels of ESD up to 10kv. PMOS IC's can successfully pass the test if the stress is applied to all inputs and outputs simultaneously; also, a toggle switch must be used instead of the lever switch to prevent arcing at high voltages. A combination of I_{DD} and functional measurements was made.

15092

DiCiaccio, C. (GTE Sylvania, Solid State Scientific)
CMOS INTEGRATED CIRCUIT.
Rept. No. E0206, Project No. 983-3050, pp. 3-11, August 4, 1976.

The evaluation conducted on the CMOS product clearly indicates that Fairchild devices are susceptible to latch-up whereas Solid State Scientific's are not.

The devices that were ESD tested show degradation in post breakdown voltage measurements. The junction degradation is not functionally detectable. The long term reliability of those devices which exhibited junction degradation is questionable. Therefore, further effort is needed at this time to investigate those devices subjected to ESD stresses.

15710

Swann, F.E. (TRW, Redondo Beach, CA)
HANDLING AND PROTECTION OF STATIC SENSITIVE ELECTRONIC PARTS AND ASSEMBLIES.
Rept. No. FIPPO-00-06A, Code No. 11982, 13 pp., May 15, 1975.

TRW Systems Group has incorporated handling and protection fabrication/inspection process procedures for static sensitive electronic parts and assemblies. Procedures specified involved the material receiving area, receiving inspection and control, testing, and storage. Special procedures for X-ray analysis, power aging and radiation screening areas also are written. Component tinning, production line assembly areas, bonding, conformal coating and general area control are also covered.

16014

Kinzig, B.J., Ravner, H. (Naval Research Laboratory, Washington, DC)
PROBLEMS ENCOUNTERED WITH ANTISTATIC PACKAGING.
NRL Memorandum Report 3873, 20 pp., November 1978.

Packaging of miniature aerospace components in antistatic polyethylene or nylon is generally considered an attractive route to eliminate major problems in their handling and storage. Although most electronic components appear compatible with antistatic packaging materials, lubricated parts, such as precision ball bearings, can apparently be adversely affected. Surfaces exposed to lubricants, for example, may become nonwetted or the lubricant may become grease-like after relatively short exposure to antistatic containers. That such packaging adversely affects lubricated parts suggests potential problems involving unwanted surface-active effects for nonlubricated parts as well.

Our recent studies indicate that the surfactant material incorporated into the packaging film may be responsible for the adverse effects observed.

16015

Gaspard, K.R., Shirk, M., Sadlak, J. (Honeywell, Avionics and Defense Systems)
UNDERSTANDING AND CONTROLLING ELECTRO-STATIC DISCHARGE.
Component Comments, Rept. No. 175, 10 pp., February 13, 1978.

This component comment addresses the areas of comprehensive cost-effective methodologies for the control of electrostatic potentials. This component comment is organized as follows: Testing/Results, major concerns of Design (Reliability, Quality, Production services, and Procurement), Control Methods, and Conclusions. Voltage sensitivity ranges were Category I, 0-170v; Category II, 171-2000v; Category III, 2001 to 15000v; Category IV, 15001 and above.

16022

Dabkowski, J. (IIT Research Institute, Chicago, IL)
INVESTIGATE FEASIBILITY OF ELECTROMAGNETIC PULSE TESTING FOR RELIABILITY SCREENING OF SEMICONDUCTOR DEVICES.
Rept. No. E6443, 50 pp., November 1978.

Tests presently used for the screening of microelectronics are generally patterned after MIL-STD-883. In addition to the accepted screening tests, it has become apparent that an additional test procedure is necessary for some technologies. MIL-M-38510 incorporates a test requirement to qualify ESD protective circuitry on the CMOS chip.

EMP tests are primarily oriented towards establishing damage thresholds and failure criteria for semiconductors exposed to an electromagnetic pulse.

Due to thermal breakdown failure effects a commonality between accepted reliability screening tests and EMP tests can be shown to exist.

16067

Pujol, H.L. (RCA, Solid State Division, Somerville, NJ)
COS/MOS ELECTROSTATIC DISCHARGE PROTECTION NETWORKS.
Rept. No. ICAN-6572, 4 pp., February 1977.

RCA's two families of CMOS devices, the standard A series (3 to 15 volts) and the high voltage B series (3 to 20 volts), are equipped with networks to protect the gate oxide of the devices against damage resulting from discharge of electrostatic energy between any two pins. Figures show the various protection networks incorporated in all COS/MOS products.

16068

Albing, B. (Hickok Electrical Instrument Company, Cleveland, OH)
COMPARATOR DETECTS POWER SUPPLY OVERVOLTAGE, CATCHES GLITCHES.
Electronic Design, Vol. 27, No. 15, p. 120, July 19, 1979.

Power-supply outputs can be monitored for intermittent overvoltage conditions by a comparator circuit that will light LED's and sound a beeper whenever a transient occurs. The circuit can be modified easily to latch the LED and beeper continuously on. This allows the circuit to run without constant monitoring.

16069

Somsak, W. (Transaction Technology Inc., Los Angeles, CA)
COPING WITH STATIC ELECTRICITY - PART XIII: ARE YOU ALSO A VICTIM OF ESD?
Evaluation Engineering, Vol. 18, No. 4, pp. 20-27, July/August 1979.

This presentation will identify potential static problem areas within the working environment. The military hardware industry more than the commercial has taken great strides to educate its contractors on electrostatic discharge. The Navy has distributed two proposed documents for review.

16074

Anon. (Reliability Sciences, Inc., Arlington, VA)
ELECTROSTATIC DISCHARGE (ESD) LIBRARY LIST.
Rept. No. 428-0036-004, Contract No. N00197-79-C-0107, 64 pp., May 10, 1979.

This document is a library list of ESD articles prepared for the Naval Ship Engineering Center. The article gives library descriptors and separately categorizes articles relating to general information, device sensitivities, and ESD control/elimination.

16074-01

Anon. (Reliability Sciences, Inc., Arlington, VA)
IDENTIFICATION OF SUPPLIERS OF ESD PROTECTIVE MATERIALS AND EQUIPMENT.
Rept. No. 428-0036-002, Contract No. N00197-79-C-0107, May 11, 1979.

Sixty-two manufacturers are identified from various sources as potential suppliers of material and equipment for the protection of sensitive devices for electrostatic discharge. Supplies are categorized as antistatic plastic, conductive plastic, and equipment or tools.

16076

Walker, R.C. (IITRI/RAC, Griffiss AFB, NY)
ELECTROSTATIC DAMAGE TO SEMICONDUCTORS.
Reliability Technology for Cardiac Pacemakers III - A Workshop Report, pp. 69-73, June 1979.

The Reliability Analysis Center (RAC) has found it convenient to classify ESD sensitive devices into three groups. These groupings should be considered generalizations, and it is cautioned that damage thresholds within generic classifications can vary widely. When in doubt, individual part types should be tested for sensitivity.

ESD-type overstress can induce latent failure mechanisms in both MOS structures and bipolar junctions which are not necessarily detectable with typical electrical tests. The overstress degrades the device, making it susceptible to failure some time after initial voltage transient in applications where voltage excursions are encountered.

16114

Pshaenich, A. (Motorola Semiconductor Products, Inc., Phoenix, AZ)
DRIVING INDUCTIVE LOADS?
Electronic Design, Vol. 25, No. 4, pp. 86-91, February 15, 1977.

Most monolithic Darlingtons have a built in (C-E) diode that is usually ignored. This diode is capable of serving as a surge suppressor for inductive loads. Because the C-E diode is usually ignored its characteristics are seldom given in spec sheets. Measurements compare favorably with several discrete rectifiers.

Fast recovery rectifiers are characterized by low reverse-recovery times. They are not particularly fast on forward recovery. Moreover, when compared to standard or even fast recovery diodes, no major difference in circuit operation can be detected for C-E diodes as a result of variation in reverse-recovery times.

16115

Graham, G.W. (Atlas Chemical Industries, Inc., Chemicals Division)
PREDICTING THE STATIC BEHAVIOR OF FIBERS AND TESTING THE EFFECTIVENESS OF ANTISTATIC AGENTS.
Textile Chemical Bulletin, 4 pp., 1952.

The test procedure described here is designed to simulate the mechanism by which fibers become charged in actual mill operations. It is based on the theory that if a textile material cannot be charged with static electricity through friction against itself and certain other materials, static should be no problem.

16116

Taylor, R. (Litton Systems, Inc., Guidance and Control Systems Division, Woodland Hills, CA)
PHYSICS OF ELECTROSTATIC CHARGE GENERATION IN INDUSTRIAL PROCESSES.
Internal Report, 16 pp., 1970.

The manufacturing process areas discussed in this paper are conformal coating/potting, hybrid facility, areas using cryogenic coolants, vapor degreasers, ultraviolet light inspection, vacuum pack processing, and Parylene coating process.

The Helmholtz effect-layer theory, Hertz effect and Van der Waals forces are used to explain charge generation. Spraying and dip coating was found not to generate electric charges. Nonoven drying causes a charge of 40 volts due to Van der Waals forces. Assemblies cured in laminar flow ovens are subject to charges when not grounded. Cryogenic cooling will cause charge generation due to the accumulation of moisture on the part with the effect of Van der Waals forces. Ultraviolet light exposure greater than 30 minutes will cause charge generation because of the Hertz effect. Charges up to 80 kilovolts can be generated when removing a polyethylene sheet from its packaging. Handling processes such as wiping with Kimwipe can cause generation of 500 volts.

16117

Clark, O.M. (General Semiconductor Industries, Inc., Tempe, AZ)
DEVICES AND METHODS FOR EMP TRANSIENT SUPPRESSION.
1975 IEEE - Electromagnetic Compatibility Symposium, 75CH1002-5 EMC, 6 pp., October 1975.

The subject of EMP (Electromagnetic Pulse) has been developed into prominence in recent years because of potential nuclear threat.

Although gas-filled spark gaps were originally designed to protect telephone apparatus from induced lightning surges they have exhibited fast turn-on characteristics when subjected to the much stronger EMP pulse. Response to laboratory simulated EMP pulses has shown that metal oxide varistors will also clamp fast rise time pulses but undergo reverse degradation upon multiple pulsing.

Both devices have been used for large system protection subject to respective limitations of short turn on times and nigh voltage clamping.

16118

Lane, C.H. (RADC, Air Force Systems Command, Griffiss Air Force Base, NY)
ELECTRICAL OVERSTRESS, "ZAP", FAILURES OF SILICON PN JUNCTIONS (U).
Job Order No. 55190000, Report No. RADC/RC-TM-71-4, 38 pp., May 1971.

This study of electrical overstress reveals the cause of the failure and explains the appearance of a "zapped" junction. It demonstrates the dependence of long pulse type zap failures on aluminum alloying and migration.

16123

Halperin, S.A. (Analytical Chemical Laboratories, Elk Grove Village, IL)
COPING WITH STATIC ELECTRICITY-PART XIV: TOPICAL ANTISTATIC PRIMER.
Evaluation Engineering, Vol 18, No. 5, pp. 56-62, September/October 1979.

Topical antistats are generally liquids which, when applied, render a material static controlled. They consist basically of two components: 1) a carrier to transport the antistatic mechanism and 2) the mechanism which performs the preventive function.

A new approach to the static problem treats static as a symptom and environmental factors as the cause of it. It follows the thought that static is a natural phenomenon and to prevent it we must counteract the natural elements that create it.

16124

Shumka, A., Miller, E.L., Piety, R.R. (Jet Propulsion Laboratory, Pasadena, CA)
FAILURE MODES AND ANALYSIS TECHNIQUES FOR CMOS MICROCIRCUITS.
1977 IEEE - Advance Technique Failure Analysis, Contract No. NAS 7-11, pp. 75-87, 1977.

The type of damage which is produced by ESD is a function of the part characteristics, voltage level and polarity energy available and the rise/fall time of the ESD pulse. After the part is soldered to the circuit board, the attached circuitry connectors and arrangement of exposed interconnections may greatly influence ESD susceptibility.

16141

Whalen, J.J., Thorn, M.L., Rastefano, E., Calactera, M.C. (State University of NY at Buffalo, Amherst, NY and Air Force Avionics Laboratories, Wright Patterson AFB, Dayton, OH)
MICROWAVE NANOSECOND PULSE BURNOUT PROPERTIES OF ONE MICRON MESFETS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 147-157.

Two dominant failure modes in overstressed MESFET's have been observed. One is the gate-to-source low resistance path (5 to 25 ohms) which frequently is correlated with metal migration (mainly gold) from the source metallization to the gate metallization. This failure mode was dominant when MESFET's failed at lower power levels as at 10 nsec. The other dominant failure mode is either a reduction in I_{DSS} or a drain-to-source short which is correlated with massive damage in the channel region between source and gate metallizations. This failure mode was dominant when MESFETs failed at this power levels as at 1.5 nsec.

16142

Branberg, G. (Hewlett-Packard Co., Loveland, CO)
ELECTROSTATIC DISCHARGE AND CMOS LOGIC.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 55-63.

This report describes a method of organizing and implementing a standardized test method for evaluating ESD susceptibility of CMOS components.

Also described are methods for detecting mechanisms of latent failure and other related phenomenon. Procedures for decapsulation and electrical probing of the die are also presented as a method of isolating the cause of failure. As shown by the results, the phenomenon of ESD is controllable and its effects statistically predictable.

16143

Yenni, D.M., Huntsman, J.R. (3M Company, St. Paul, MN)
THE DEFICIENCIES IN MILITARY SPECIFICATION MIL-B-81705: CONSIDERATIONS AND A SIMPLE MODEL FOR STATIC PROTECTION.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 45-54.

Military Specification MIL-B-81705 has been relied on to define static protective materials. Advancing technology has made its methods antiquated.
The single most important characteristic of any packaging material is its conductivity. To fully characterize a film as being static protective, all that is needed is a resistivity test. Existing ASTM test procedures can be used.

16144

McCullough, D.T., Lane, C.H., Blore, R.A. (RADC, Griffiss AFB, NY)
RELIABILITY OF EOS SCREENED GOLD DOPED 4002 CMOS DEVICES.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 36-40.

A proposed electrical overstress (EOS) test method for MIL-STD-883, "Test Methods and Procedures for Microelectronics," was applied as a characterization and screening procedure to a population of gold doped 4002 CMOS devices. To evaluate the possibility of subsequent reliability degradation of devices passing the screen, a high temperature accelerated life test was performed on screened and unscreened devices. For screening, a voltage pulse of sufficient magnitude to fail about 3% of the parts was applied. No significant differences were detected between the failure rates of the screened and unscreened device populations.

16145

Madzy, T.M., Price, L.A. II (IBM Corp., Systems Products Division, Endicott, NY)
MODULE ELECTROSTATIC DISCHARGE SIMULATOR.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 36-40.

Under certain conditions electrostatic discharge (ESD) can cause catastrophic failure in both bipolar and field effect transistor (FET) devices. This paper presents a test technique and describes a testing device that simulates ESD produced by human handling.

16146

McMahon, E.J., Bhar, T.N. (Reliability Sciences, Inc. Arlington, VA) and Oishi, T. (Naval Sea Systems Command, Washington, DC)
PROPOSED MIL-STD AND MIL-HDBK FOR AN ELECTROSTATIC DISCHARGE CONTROL PROGRAM - BACKGROUND AND STATUS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 27-35.

Many electrical and electronic devices and components are sensitive to Electrostatic Discharge (ESD). However, ESD controls generally have not been widely implemented by either industry or government. This lack of controls has resulted in increased costs, decreased equipment reliability and increased equipment downtime. To address these problems the Naval Sea Systems Command, under DoD Project Nos. RELI-014 and RELI-012 is developing a military standard and handbook on implementation of ESD control programs. Background, content and status of these documents are presented. Additionally, ESD areas requiring further work are discussed.

16147

DerMarderosian, A., Rideout, L. (Raytheon Co., Equipment Divison, Sudbury, MA)
THE GENERATION OF ELECTROSTATIC CHARGES IN SILICONE ENCAPSULANTS DURING CYCLIC GASEOUS PRESSURE TESTS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 22-26.

Sporadic electrical signal losses were noted during system qualification testing in a cyclic gaseous pressure/vacuum environment. There were electrical timing disturbances noted at depressurization.

A static charge hypothesis was developed that involved movement of the potting compound. During pressurization, gas bleeds into areas of poor adherence between the module frame and silicon encapsulant. During depressurization the entrapped gas will stress the potting, causing a separation at the bonded interface, thereby generating a charge.

16148

Halperin, S.A. (Analytical Chemical Laboratories, Elk Grove Village, IL)
STATIC CONTROL USING TOPICAL ANTISTATS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 13-21.

Triboelectric static charges can be prevented by using properly selected topical antistats. Utilizing the concept of Environmental Static Control (ESC), the burden of a company's overall static control program can be shifted from the line employee to a management team made up of operations and maintenance personnel. If proper instrumentation is employed, constant performance feedback and detailed analysis are available. As a result, the optimal return in static prevention, at the lowest possible cost can be achieved.

16149

Storm, D.C. (Aerospace Corp., El Segundo, CA)
CONTROLLING ELECTROSTATIC PROBLEMS IN THE FABRICATION AND HANDLING OF SPACECRAFT HARDWARE.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 4-6.

This paper discusses the sources of electrostatic discharge (ESD) and the detailed requirements for protecting electronic parts and assemblies that may be sensitive to ESD. The procedures could be employed on future space projects to ensure that proper safeguards are taken during manufacturing and testing to protect space flight hardware from ESD hazards.

16150

Briggs, C., Jr. (Charles Stark Draper Laboratory, Inc., Cambridge, MA)
ELECTROSTATIC CONDUCTIVITY CHARACTERISTICS OF WORKBENCH - TOP SURFACE MATERIALS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 7-12.

Testing has been conducted at The Charles Stark Draper Laboratory, Inc. (CSDL) on several typical or potential bench-top materials. The tests consisted of charging bench-top samples and then discharging them to a ground. All samples exhibited an exponential decay of voltage with time. The only exceptions were vacuum-baked samples of melamine and Benalux-type materials. The author is also certain that pink poly would be an exception if it were vacuum baked. All samples produced a visible static discharge arc when the charged test specimen was grounded.

16151

Uetsuki, T., Mitani, S. (Hitachi, Ltd., Production Engineering Research Laboratory, 292 Yoshida-Machi, Totsuka-Ku, Yokohama 244, Japan)
FAILURE ANALYSIS OF MICROCIRCUITS SUBJECTED TO ELECTRICAL OVERSTRESS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 88-96.

The differential input pair transistors of an operational amplifier are susceptible to severe damage from EOS/ESD.

Typical failure modes of TTL IC's include degradation of the I-V characteristic or short of the input protection diode.

EOS/ESD can easily cause degradation of the electrical characteristics or catastrophic damage.

16152

King, W.M. (Electromagnetic Compatibility Advisor, Santa Monica, CA)
DYNAMIC WAVEFORM CHARACTERISTICS OF PERSONNEL ELECTROSTATIC DISCHARGE.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 78-87.

This paper briefly summarizes a study that was initiated to advance knowledge of Personnel Electrostatic Discharge (ESD) by developing descriptions of the "Source" waveforms resulting from the ESD of personnel associated with operation of Electronic Data Processing (EDP) systems. The study was extended to include measurements of the waveforms of ESD from (and through) mobile furnishings and the ESD of personnel through various handheld metallic objects that were intervening in the discharge path. The conceptual direction of this effort was aimed toward eventual development of ESD test simulation equipment and methodology, based on matching the waveforms found during the primary "source" evaluation effort through to the design of the test simulation equipment. From the standpoint of systems susceptibility performance, the conclusions provided by this effort have achieved good correlation in terms of systems operation in active-use situations. Although directed toward systems-susceptibility considerations, the waveform results of this study could easily be applied to equivalent circuit models for purposes of evaluating semiconductor device/component ESD damage.

16153

Rutherford, D.H. (Raytheon Company, Electromagnetic Systems Divison, Goleta, CA)
Perkins, J.F. (Hi-Rel Laboratories, Inc., Monrovia, CA)
EFFECTS OF ELECTRICAL OVERSTRESS ON DIGITAL BIPOLAR MICROCIRCUITS AND ANALYSIS TECHNIQUES FOR FAILURE SITE LOCATION.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 64-77.

A large percentage of the microcircuits submitted for failure analysis that are actually defective have been found to be damaged by electrical overstress. It is not unusual to see 60 to 75% of actual failures the result of some sort of overstress conditions. Prior reports of failures of some digital microcircuits gives the impression that certain families of devices have different damage susceptibility levels. This paper describes a series of stress tests performed on several digital microcircuits and the failures that were induced. Procedures used for failure analysis of the damaged microcircuits are discussed.

16154

Madison, J.A. (Westinghouse Electric Corp., Baltimore, MD)
THE ANALYSIS AND ELIMINATION OF EOS INDUCED SECONDARY FAILURE MECHANISMS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 205-209.

When performing failure analysis at the system or printed wiring board level for a high reliability program, any associated part that could have been overstressed is identified and removed. The procedure is summarized and the circuit analysis is illustrated by several examples. A summary of the secondary part type replacements and the related overstress characteristics are given. The procedure has been successful in preventing system level failures from this cause over a five-year period involving 300 printed circuit boards and 200 power supply assemblies that contain 10,000 multichip hybrid packages.

16155

Cabayan, H.S., Deadrick, F.J., Martin, L.C., Mensing, R.W. (Lawrence Livermore Laboratory, Livermore, CA)
STATISTICAL FAILURE ANALYSIS OF MILITARY SYSTEMS FOR HIGH-ALTITUDE EMP.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 198-204.

A study of general problems of dealing with uncertainties and their impact on failure analysis in assessment of EMP effects on military systems has suggested a probabilistic approach. Major uncertainties arise in both the interaction and coupling and susceptibility phases of assessment studies. A probabilistic approach, as outlined in this paper, can accommodate all sources of uncertainties. Although propagation of uncertainties by analytical methods is possible for very simple systems, the approach suggested is based on Monte Carlo methods and uses available computer programs such as FAST and NET-2. The results of the two simple experiments demonstrate the validity of the tools used and shows the potential usefulness for more complex systems.

16156

Clark, O.M. (General Semiconductor Industries, Inc., Tempe, AZ)
ELECTROSTATIC DISCHARGE PROTECTION USING SILICON TRANSIENT SUPPRESSORS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 193-197.

The vulnerability of a semiconductor device increases as the slope of the transient voltage wavefront increases. The micro-structures characteristic of new semiconductor technology are very fragile and are easily destroyed with the fast rise-time transients originating from electrostatic discharge (ESD). A new silicon transient suppressor structure has been developed specifically for clamping the fast rise-time of ESD and represents more than an order of magnitude improvement over conventional silicon suppressors. Effectiveness of both of these types of suppressors is evaluated and reported in this paper.

16157

Minear, R.L., Dodson, G.A. (Bell Telephone Laboratories, Reading, PA)
THE PHANTOM EMITTER - AN ESD - RESISTANT BIPOLAR TRANSISTOR DESIGN AND ITS APPLICATIONS TO LINEAR INTEGRATED CIRCUITS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 188-192.

The immunity of an NPN IC transistor to ESD damage can be markedly improved by simple design changes. The resulting "phantom emitter" transistor used in bipolar op-amp circuits makes their inputs much more damage resistant. The "phantom emitter" diffusion is shorted to the normal base contact by metal and plays no part in normal device operation.

16158

Petrizio, C.J. (RCA Solid State Division, Somerville, NJ)
ELECTRICAL OVERSTRESS VERSUS DEVICE GEOMETRY.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 183-187.

Each section of a CMOS quad two-input NOR gate was independently stressed. The resulting failures can be related to device geometry. Review of the test data indicates excessive quiescent leakage (I_{SS}). The failures occurred farthest from the V_{SS} contact. The higher input diode resistance results in a higher voltage drop and increased dissipation. An additional P-well contact was proposed to reduce the voltage drop.

16159

Soden, J.M. (Sandia Laboratories, Albuquerque, NM)
THE DIELECTRIC STRENGTH OF SILICON DIOXIDE IN A CMOS TRANSISTOR STRUCTURE.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 176-182.

It is important to know if the processes required to fabricate the MOS device structure such as oxide etch and regrowth and topographical features such as edges and steps have significant effect upon the SiO_2 gate oxide maximum dielectric strength. Also important to know is how gate oxide defects in the MOS structure affect this maximum dielectric strength.

The primary breakdowns occurred at topographical edges at the gate/field oxide interface and the secondary distribution of breakdowns at random locations in the central region of the gate. The maximum dielectric strength in the primary distribution is within about .5MV/cm of that reported for uniform thickness SiO_2 in capacitor studies.

16160

Teng, T.T., Hart, A.R., McKenna, A. (Hewlett-Packard Co., Corvallis Division, Corvallis, OR)
SUSCEPTIBILITY OF LSI MOS TO ELECTROSTATIC DISCHARGE AT ELEVATED TEMPERATURE.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 168-175.

An investigation of random failures during 125°C burn-in of LSI MOS Memory devices led to a study of the effects of elevated temperature on ESD susceptibility. An experiment was conducted on the ESD susceptibility versus temperature on MOS LSI devices including PMOS, NMOS, and CMOS devices produced by three IC manufacturers. A reduction in ESD failure voltage (V_f) is found at 125°C compared with room temperature levels. An explanation of bulk doped silicon resistivity variation in the input junction protection diode versus temperature combined with processing nonuniformities is offered and supported with a simplified power and current model and physical failure analysis.

This phenomenon affects high temperature testing used for life test, activation energy determination, receiving inspection, outgoing screening, Hi Rel and military specification testing and MOS applications in extreme temperature environments.

16161

Formanek, V.C. (IIT Research Institute, Chicago, IL)
DAMAGE RESPONSE OF SELECTED INTERFACE INTEGRATED CIRCUITS TO A SIMULATED EMP WAVEFORM.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 158-167.

The damaging effects of a 20 MHz damped sinusoid on 18 types of powered devices are presented. Failure levels are given in terms of peak currents and voltages. The three most sensitive devices are also modeled in terms of failure energy and failure modes are presented.

16174

Kusnezov, N., Smith, J.S. (Lockheed, Palo Alto Research Labs, Palo Alto, CA)
MODELING OF ELECTRICAL OVERSTRESS IN SILICON DEVICES.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 133-139.

This paper describes qualitative results of the work to date and is intended to show only general trends. A quantitative analysis of the junction burnout problem remains to be analyzed, and these results will appear in a later paper. The justification for going to more than a simple one-dimensional analysis is described. The extension of the 1-D to 2 or 3-D analysis is briefly explained and has been restricted to what has been learned from the viewpoint of power dissipation. Folding-in temperature effects serve generally to wash out the basic results that are best illustrated by studying the initial power dissipation.

16200

Baruah, A., Budenstein, P.P. (Auburn University, Auburn, AL)
AN ELECTROTHERMAL MODEL FOR CURRENT FILAMENTATION IN SECOND BREAKDOWN OF SILICON-ON SAPPHIRE DIODES.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 126-132.

Second breakdown is generally regarded as one of the principal failure modes of silicon electronic components.

The susceptibility of a particular device to second breakdown depends upon device geometry, spacings, contours, doping levels and heat sinking. The filamentation process involves large currents in a small region of space in short intervals. In modeling the high current pulse effects on P-N junctions, there is an interval when devices are ballasted by the junction voltage; however, when the temperature of the junction becomes high enough the voltage drops precipitously and the filament evolves rapidly.

16201

Schnetker, T.R. (Gould Inc., OSD, Cleveland, OH)
HUMAN FACTORS IN ELECTROSTATIC DISCHARGE PROTECTION.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 122-125.

The heart of an effective ESD control program is commitment to the program by production operators throughout the facility. The unseen nature of electrostatic damage makes it much more difficult to control than the usual quality defects. Consideration of small work group behavior in the design of electrostatic control programs will lead to real acceptance of electrostatic work rules.

16202

Blackburn, D.L., Berning, D.W. (National Bureau of Standards, Electron Devices Division, Washington, DC)
REVERSE-BIAS SECOND BREAKDOWN IN POWER TRANSISTORS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 116-121.

Second breakdown in bipolar transistors has been divided into two regimes, forward and reverse. The phenomenon of thermal instability and its relationship to forward bias second breakdown is well understood; the events preceding reverse bias second breakdown are not well understood. Data curves show that the voltage at which second breakdown occurs decreases as the reverse bias increases. This supports the theory that the focusing of current to the center of the emitter fingers during turnoff is the mechanism that leads to reverse bias second breakdown.

16204

Whalen, J.J. (SUNY at Buffalo, Amherst, NY) and Domingos, H. (Clarkson College of Technology, Potsdam, NY)
SQUARE PULSE AND RF PULSE OVERSTRESSING OF UHF TRANSISTORS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, 7 pp.

Square and RF pulse overstress data for bipolar UHF transistors are compared. For pulses incident upon the base-emitter terminals the pulses with lowest energy required to cause device failure were reverse polarity square pulses. The comparison indicates that a data format of absorbed pulse energy up to time of failure vs time to failure is well suited for comparing data produced by different types of signals.

16206

Ward, A.L. (Harry Diamond Laboratories, Adelphi, MD)
DOPING PROFILES AND SECOND BREAKDOWN.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 109-115.

With the understanding of second breakdown, one should be able to design devices less susceptible to burnout. The electrothermal computer program has been used to study second breakdown in linearly graded, double- and single-sided abrupt and diffused junction diodes. Tentative design principles are given.

16207

Anand, Y. (Microwave Associates, Inc., Burlington, MA) and Morris, G., Higgins, V. (U.S. Army Electronics Technology and Device Laboratory, ERADCOM, Fort Monmouth, NJ)
ELECTROSTATIC FAILURE OR X-BAND SILICON SCHOTTKY BARRIER DIODES.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 97-103.

A recently developed platinum-silicon Schottky barrier diode was found to be least sensitive to burnout by electrostatic discharge.

Electrostatically burned-out diodes from both natural and circuit simulation techniques exhibited failure points at the periphery of the diode junction similar to that observed for RF burnout depending on junction parameter. A strong correlation exists between electrostatic and RF burnout of Schottky barrier diodes.

16208

Moon, M.G. (Harris Semiconductor, Products Division, Melbourne, FL)
ESD SUSCEPTIBILITIES OF HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS.
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 104-108.

The operational amplifier, sample hold amplifier and comparator all share a similar input stage configuration - the bipolar differential input stage. If we apply an ESD pulse to either the inverting or non-inverting input with the other grounded, then there is a conduction path involving both a forward and reverse biased P-N junction.

A second classification of analog circuits is CMOS analog switches and multiplexers. Degradation may occur in three areas: switch cell; address cell; and decode. Switch cell degradation can be both MOS dielectric and P-N junction damage that may result in input-output off state isolation degradation as a result of PN junction damage or solid DC voltages and switching waveforms, depending upon damage location in the MOS dielectric. The address cell is susceptible only to MOS dielectric structure damage destroying the input MOSFET gate. The decode degradation, though an internal circuit structure because of small geometry MOSFETs, can be compromised through the capacitive divider model.

16226

Biddle, J.G. (Hughes Aircraft Company)
AIR IONIZING GRIDS - A COMPARATIVE ANALYSIS.
Internal Report, 6 pp., October 19, 1979.

Tests on air ionizing grids were conducted to determine which grids would reduce to less than 100v a static charge of 15kv. The companies that submitted their products to independent testing were Scientific Enterprises, Static Inc., Simco and Westcorp. The laminar flow hood used in the experiment was a vertical down flow type made by Dexon Corp.

16230

Lee, T.W. (Motorola Incorporated)
TRANSIENT DAMAGE IN POWER TRANSISTORS.
Proceedings of Advance Techniques in Failure Analysis, pp 130-135, 1979.

A significant percentage of power transistor failure analyses reveal electrically damaged devices which were properly constructed and correctly applied. When extensive background data is present, transient records are generally absent, due to their expense of collection. Under these circumstances, the analyst must logically conclude that the device was damaged by a non-repetitive transient event. A systematic study was undertaken to identify correlations between physical appearance of the damaged area and electrical quantities involved in its generation. It was found that peak and total transient energy correlated roughly to damage area size, transistor ratings, and resistance. Power transistors were shown to be resistant to successive damaging pulses below a certain threshold level. In transistors heavily damaged by the passage of large amounts of current following a transient, these subcritical damage areas may be the only conclusive analytical evidence present.

16267

Kahn, S.R. (IIT Research Institute, Chicago, IL)
EFFECTS OF EMP TESTING ON SEMICONDUCTOR LONG TERM RELIABILITY.
Rept. No. DNA 4468F, Contract No. DNA 001-76-C-0243, NWED Subtask R99QAXEB097-61, 80 pp., November 1977.

The objective of this report was to determine the effects of stressing semiconductor devices with EMP-like transients. The effects of EMP stressing on the devices was assessed by comparing the observed failure rates of the various samples under these accelerated life test conditions.

16285

Cooke, J.L., Duncan, D.E., Schwarz, J.J., Skinner, L.H. (Boeing Aerospace Company, Seattle, WA and BDM Corporation, Albuquerque, NM)
USERS MANUAL FOR SUPERSAP 2.
Rept. No. AFWL-TR-75-70, Contract No. F29601-74-C-0008, D224-13047-2; BDM/A-120-74-TRR1, 208 pp., March 1976.

This report presents user information for the computer code Supersap 2. Supersap 2 is a data storage and retrieval program. It is designed to manipulate data from two large data bases in support of EMP susceptibility threshold analysis. The component data base contains data on approximately 86,000 electronic component types. The system description data base is user defined. Supersap 2 uses a command language to provide user control of a variety of data manipulations.

16302

McAteer, O.J. (Westinghouse Electric Corporation, Baltimore, MD)
AN EFFECTIVE ESD AWARENESS TRAINING PROGRAM
IITRI - EOS/ESD Symposium, Sept. 1979, RAC Catalogue No. EOS-1, pp. 1-3.

The need for electrostatic discharge (ESD) awareness on the part of personnel at typical electronic manufacturing facilities is described. Some of the underlying reasons for intuitive disbelief in the static problem are discussed as well as the consequences of nonawareness. The development of an effective training program and proper manner of delivery to the appropriate personnel is presented.

16376

Adair, R.P. (Unitrode Corporation)
TRANSIENT-VOLTAGE SUPPRESSORS SUIT PC-BOARD PROTECTION NEEDS.
EDN, Vol. 24, No. 15, pp. 105-109, August 20, 1979.

When transient voltages occur, system voltages and currents can surge to levels many times greater than their steady state values, permanently damaging semiconductor components. Zener transient-voltage suppressors offer a simple inexpensive method of shunting aside these transients before they reach sensitive components.

16377

Formanek, V.C., Mindel, I.N. (IIT Research Institute, Chicago, IL)
EMP TO ESD VZAP DATA CONVERSION AND CONSIDERATIONS.
30 pp., 1979.

The physical damage mechanisms for ESD and EMP are basically the same. The principal differences are the voltage source and coupling mechanism resulting in different driving voltage waveforms and source impedances.

The principal objective of this report is to find common or equating parameters between EOS and ESD.

16378

Myers, S. (Honeywell, Aerospace Division, St. Petersburg, FL)
A TOTAL APPROACH TO ELECTROSTATIC PROTECTION IN THE PRODUCTION ENVIRONMENT.
1977 Packaging, Handling, and Transport Symposium, Defense Preparedness Association, 16 pp., 1977.

Static electricity can never be eliminated but it can be controlled. Today electronic environment demands that each and every packaging engineer accept his responsibility to see that electrostatic discharge is properly addressed.

This article provides information that will aid him in meeting this responsibility.

16379

Huntsman, J.R. (3M Static Control Systems, St. Paul, MN)
SELECTED REFERENCES TO THE THEORY AND EXPERIMENT OF STATIC ELECTRICITY AND ELECTROSTATIC DAMAGE TO ELECTRONIC DEVICES.
16 pp., November 1979.

This is a list of references compiled by 3M Static Control Systems relating to the theory and experiment of static electricity.

17013

Storm, D.C. (Aerospace Corp., El Segundo, CA)
STANDARD FOR HANDLING OF ELECTROSTATIC PARTS AND ASSEMBLIES.
Rept. No. TOR-0079 (4902-04-2, Contract No. F04701-78-C-0079, 20 pp., February 15, 1979.

This document establishes common procedures and precautionary measures for the protection of ESD sensitive devices and components. Work station, clothing, protective packaging, and design documentation are covered in detail.

17075

Sabaroff, S. (Hughes Aircraft Company, El Segundo, CA)
STATIC ELECTRICITY CASE HISTORIES.
Spacecraft Electromagnetic Interference Workshop held at Jet Propulsion Lab., 33-402, pp. 203-214, February 1968.

The major sources of static charge are on or near the earth. The list could include fuel handling, plastics, rocket engine charging, precipitation, friction, lightning, booster separation and many others.

Static charge buildup on spacecraft and humans has been investigated throughout the industry. Transistor and SCR failures have also been related to static effects.

17076

Rogers, P.R. (General Electric Company, Philadelphia, PA)
TRANSIENT COMPATIBILITY MEASUREMENTS IN SPACECRAFT.
Spacecraft Electromagnetic Interference Workshop held at Jet Propulsion Lab., 33-402, pp. 197-202, February 1968.

The capability of measuring broadband and narrowband frequency domain voltages has existed for many years. In any given system the fundamental and most spurious frequencies are known. The source of interfering transients is usually the operation of relays, tuning components, and other high current level changes mostly on main power buses.

17077

Whittlesey, A.C. (Jet Propulsion Laboratory, Pasadena, CA)
SPACECRAFT INTERFACE CIRCUITRY SENSITIVITY ANALYSIS.
Spacecraft Electromagnetic Interference Workshop held at Jet Propulsion Lab., 33-402, pp. 171-184, February 1968.

The study presented concerns Mariner/Mars Spacecraft. This study was done after the spacecraft was conceived, designed and launched into space. It was limited to intersubsystem problems because of the way the JPL builds.

17078

Schenker, B. (Lockheed Missiles & Space Co., Sunnyvale, CA)
TRANSIENT MEASUREMENTS IN AEROSPACE VEHICLES.
Spacecraft Electromagnetic Interference Workshop held at Jet Propulsion Lab., 33-402, pp. 163-169., February 1968.

Two methods of transient voltage measurement at selected critical points in an aerospace vehicle are described in this paper. These measurements are for the purpose of injecting 6dB higher voltages into aerospace vehicles to demonstrate compliance with specification MIL-E-6051C. Both methods have given positive results in attaining the required objective, but the memory voltmeter/oscillograph combination is preferred because of its simplicity. This latter method is planned to be used in future EMI system compatibility tests.

17079

Butts, A.J., Ellisor, R.W. (Martin Marietta Corp., Denver Division, Denver CO)
CONTROL OF ELECTROSTATIC INTERFERENCE IN SPACECRAFT.
Spacecraft Electromagnetic Interference Workshop held at Jet Propulsion Lab., 33-402, pp. 215-220, February 1968.

A study of various electrostatic phenomena will show that both an insulating material and a charging mechanism are always involved. The charging mechanism involves motions of particles, liquids, gases, or in some instances the insulating material itself. There is one factor that can be controlled to some degree: the resistivity of the materials exposed to these charging mechanisms. If conductive materials were always used no electrostatic charge could be developed, and a situation that could be called electrostatic compatibility (ESC) would exist.

17080

Hoffart, H.M. (General Electric Co., Valley Forge Space Technology Laboratories, King of Prussia, PA)
THE CONCEPT OF SINGLE-POINT GROUNDING.
Spacecraft Electromagnetic Interference Workshop, JPL Technical Memorandum 33-402, pp. 221-230, February 1968.

Grounding concepts must be designed on a system level rather than on an individual equipment basis because of interface requirements. Effective grounding is not difficult to achieve if properly approached within the discipline of electromagnetic compatibility. The single-point grounding concept is shown to exhibit advantages if effectively implemented. The use of litzwire due to the interweaving of insulated strands will display a low impedance characteristic up to the low MHz area of the frequency spectrum. At the subsystem end, litzwire is used to separately reference the signal and static grounds.

SECTION 8

STANDARDS

Handbooks, Specifications and Standards Specifying Test Methods and Controls for Protection of Electrical and Electronic Parts, Assemblies and Equipment Against Electrostatic Discharge:

U.S. GOVERNMENT DOCUMENTS

DOD-HDBK-263	Electrostatic Discharge Control Handbook for Electrical and Electronic Parts, Assemblies and Equipment Requirement for the Electrostatic Discharge Protection of Electronic Components and Assemblies
NAVORD OD 46363	Requirements for the Electrostatic Discharge Protection of Electronic Components and Assemblies
DOD-STD-1686	Electrostatic Discharge Control Program for Electrical and Electronic Parts, Assemblies and Equipment
FED-STD-101B	Preservation, Packaging and Packing Materials, Test Procedures; Test Method 4046 Electrostatic Properties of Materials
MIL-STD-129H	Marking for Shipment and Storage
MIL-STD-758B	Packing Procedures for Submarine Repair Parts
MIL-STD-883B	Test Methods and Procedures for Microelectronics; Test Method 30XX Electrostatic Discharge Sensitivity (Proposed)
MS-90363G	Box, Fiberboard, with Cushioning for Special, Minimum Cube Storage and Limited Reuse Applications
MIL-B-117	Bags, Sleeves and Tubing, Interior Packaging
MIL-S-19491	Semiconductor Devices, Packaging of
MIL-M-38510	Microcircuits, General Specification for
MIL-M-55565A	Microcircuits, Packaging of
MIL-B-81705B	Barrier Materials, Flexible, Electrostatic-Free, Heat Sealable
MIL-P-81997A	Pouches, Cushioned, Flexible, Electrostatic-Free, Reclosable, Tranparent

U.S. GOVERNMENT DOCUMENTS (Cont'd)

PPP-C-1842	Cushioning Material, Plastic, Open Cell (For Packaging Application)
NAVSUP/SPEC STD Form 36, Contract Requirement G-64	Packaging Instructions for Electromagnetic and Electrostatic Protection

FOREIGN GOVERNMENT DOCUMENTS

Defense STD-59-98	Handling Procedures for Static Sensitive Devices

INDUSTRY DOCUMENTS

AATCC

134-1975	Test Method for the Electrostatic Propensity of Carpets

ANSI

47 (Secretariat) 707-Draft	Test Method for Electronic Devices Sensitive to Electrostatic Discharge
Z41.3	Conductive Safety-Toe Footwear: Section 5, Conductivity

ASTM

D257-78	D-C Resistance of Conductive of Insulating Materials
D991-75	Test Method for Rubber Property-Volume Resistivity of Electrically Conductive and Antistatic Material
D2679-78	Test Method for Electrostatic Charge
D3509-76	Test Method for Electrostatic Field Strength Due to Surface Charges

EIA (JEDEC)

RS-471	Attention Symbol and Label for Electrostatic Devices

NAS

NAS-853	Field Force, Protection for

INDUSTRY DOCUMENTS (Cont'd)

NFPA

No. 56A	Inhalation Anesthetics: Section 46 Reduction in Electrostatic Hazard
No. 77	Static Electricity

UL

217	Single and Multiple Station Smoke Detectors: Section 36 Static Discharge Test

U.S. GOVERNMENT DOCUMENTS

Specification Sales (3FRSBS)
Bldg. 107, Washington Navy Yard
General Services Adminstration
Washington, DC 20407

FED-STD-101B
PPP-C-1842

Commanding Officer
Naval Publications and Form Center
5801 Tabor Avenue
Philadelphia, PA 19120

DOD-HDBK-263	MIL-B-117
NAVORD OD-46363	MIL-S-19491
DOD-STD-1686	MIL-M-55565A
MIL-STD-129H	MIL-B-81705B
MIL-STD-758B	MIL-P-81997A
MIL-STD-883B	NAVSUP/SPEC STD Form 36
MS-90363G	Contract Requirement G-64

DOD-HDBK-263: Electrostatic Discharge Control Handbook for Electrical and Electronic Parts, Assemblies and Equipment

This handbook provides guidelines for the establishment of an Electrostatic Discharge (ESD) Control Program in accordance with DOD-STD-1686. This document is applicable to the protection of electrical and electronic parts from damage due to ESD.

NAVORD OD 46363: Requirements for the Electrostatic Discharge Protection of Electronic Components and Assemblies

This ordinance document covers the general and detail requirements for the electrostatic discharge protection of electronic components and assemblies.

DOD-STD-1686: Electrostatic Discharge Control Program for Electrical and Electronic Parts, Assemblies and Equipment

This standard provides direction for the establishment and implementation of an Electrostatic Discharge (ESD) Control Program for any activity that designs, tests, inspects, services, manufactures, processes, assembles, installs, packages, labels, stores or stows or otherwise handles electrical or electronic parts susceptible to damage caused by static electricity.

FED-STD-101B: Preservation, Packaging and Packing Materials Test Procedures; Test Method 4046: Electrostatic Properties of Materials

The test method in this standard describes the procedures to use for testing the electrostatic properties of various materials.

MIL-STD-129H: Marking for Shipment and Storage

Paragraph 5.4.38 of this standard specifies the marking requirements of unit, intermediate and exterior packs of sensitive electronic (ESDS) items.

MIL-STD-758B: Packing Procedures for Submarine Repair Parts

Appendix C of this standard covers protection for sensitive electronic items such as, but not limited to, diodes, transistors, integrated circuits, and equipments incorporating such items which are susceptible to damage from electrostatic, electromagnetic, or both field forces.

MIL-STD-883B: Test Methods and Procedures for Microelectronics; Test Method 30XX: Electrostatic Discharge Sensitivity (Proposed)

The test method in this standard establishes the means for measuring the electrostatic discharge sensitivity for all microcircuits, which will be used to determine the particular sensitivity class and the appropriate packaging requirements for each device type.

MS-90363G: Box, Fiberboard, with Cushioning for Special, Minimum Cube Storage and Limited Reuse Applications

Dash Nos. 6, 7, and 8 of this standard specify the packaging and marking requirements of electrostatic sensitive devices.

MIL-B-117: Bags, Sleeves and Tubing, Interior Packing

This specification covers bags, sleeves and tubing, and interior packing for the preservation-packaging, field force protection (shielding), packing and container marking of electrical and electronic devices.

MIL-S-19491: Semiconductor Devices, Packaging of

This specification covers the requirements for the preservation-packaging, field force protection (shielding), packing and container marking of all types of semiconductor devices (such as diodes and transistors).

MIL-M-38510: Microcircuits, General Specification for

Slash sheets covered under this specification contain VZAP requirements for CMOS and MOS integrated circuits.

MIL-M-55565A: Microcircuits, Packaging Of

This specification covers the requirements for the preservation-packaging, field force protection (shielding), packing and container marking of all types of microcircuits.

MIL-B-81705B: Barrier Materials, Flexible, Electrostatic-Free, Heat Sealable

This specification covers opaque and transparent heat sealable, electrostatic-free, flexible, barrier materials for the packaging of missiles, explosive powered and electro-sensitive devices, microcircuits, semiconductors and thin film resistors.

MIL-P-81997A: Porches, Cushioned, Flexible, Elecrostatic-Free, Reclosable, Transparent

This specification covers the requirements for flexible electrostatic-free reclosable transparent porches designed for shielding, packaging and storage of static-sensitive electronic devices.

PPP-C-1842: Cushioning Material, Plastic, Open Cell (For Packaging Applications)

This specification covers the requirements for Plastic Open Cell Cushioning Material designed for shielding, packaging and storage of static-sensitive devices.

NAVSUP/SPCC Form 36, Contract Requirement G-64: Packaging Intructions For Electromagnetic and Electrostatic Protection

This contract clause specifies the packaging instructions for the protection of field forces sensitive items.

FOREIGN GOVERNMENT DOCUMENTS

Ministry of Defense
Directorate of Standardization
First Avenue House
High Holborn
London WC1V 6HE

Defense Standard 59-98; Handling Procedures for Static Sensitive Devices

This standard provides guidance relating to the handling, identification and packaging of static sensitive devices.

INDUSTRY DOCUMENTS

American Society for Textile Chemists and Colorists
AATCC Technical Center, P.O. Box 12215
Research Triangle Park, NC 27709

AATCC Test Method 134-1975: Electrostatic Propensity of Carpets

This test method is designed to assess the static propensity of carpets by controlled laboratory simulation of conditions which may be met in practice, and more particularly, with respect to those conditions which are known from experience to be strongly contributary to excessive accumulation of static charges.

American National Standards Institute
1430 Broadway
New York, NY 10018

ANSI Test Method 47 (Secretariat) 707 (Proposed): Electronic Devices Sensitive to Electrostatic Discharges

This test method is designed to determine which electronic devices are sensitive to electrostatic discharge to the degree that they require special handling precautions.

ANSI Standard 241.3-1976; Conductive Safety-Toe Footwear

This standard provides the requirements for the design of conductive safety-toe footwear which protects against the hazards of the buildup of static electricity.

American Society of Testing and Materials
1916 Race Street
Philadelphia, PA 19103

ASTM Test Method D257-58: D-C Resistance or Conductance of Insulating Materials

This test method covers direct-current procedures for the determination of d-c insulation resistance, volume resistance, volume resistivity, surface resistance and surface resistivity of electrical insulating materials or the corresponding conductances or conductivities.

ASTM Test Method D991-75: Rubber Property-Volume Resistivity of Electrically Conductive and Antistatic Products

This test method covers the determination of volume resistivity of rubbers used in electrically conductive and antistatic products.

ASTM Test Method D2679-78: Electrostatic Charge

This test method covers the determination of the amount of electrostatic charge present on or in a specimen or of the electrostatic charge transferred between two material objects upon contact.

ASTM Test Method D3509-76: Electrostatic Strength Due to Surface Charges

This test method covers the determination of the value of electrical field strength at and near a variety of objects such as metal surfaces at high voltages and insulating bodies with electrostatic charge.

Electronic Industries Association
2001 Eye Street
N.W. Washington, DC 20006

EIA Standard RS-471: Attention Symbol and Label for Electrostatic Sensitive Devices

This standard provides a distinctive caution symbol and label to be used to identify those electronic devices that require special handling to prevent damage due to electrostatic discharge.

National Standards Association
1321 Fourteenth Street N.W.
Washington, DC 20005

NAS 853: Field Force, Protection For

This standard provides for the protection of items, components and assemblies which may be damaged by field forces (electrostatic, electromagnetic, magnetic or radioactive) encountered in nonoperating environment.

National Fire Protection Association
470 Atlantic Ave
Boston, MA 02210

NFPA Standard 56A: Inhalation Anesthetics; Section 46: Reduction in Electrostatic Hazard

Section 46 of this standard provides the requirements to reduce the possibility of electrostatic spark discharges, with consequent ignition of flammable gases in anesthetizing locations.

NFPA Standard 77: Static Electricity

This standard provides recommended practices that assist in reducing the fire hazard of static electricity by presenting a discussion of the nature and origin of static charges, the general methods of mitigation and recommendations in certain specific operations for its dissipation.

Underwriter's Laboratory
383 Pfingsten Road
Northbrook, IL 60062

UL Code 217: Single and Multiple Station Smoke Detectors; Section 36: Static Discharge Test

Section 36 of this code provides a test to determine if smoke detector units are sensitive to electrostatic discharges.

APPENDIX

ADDITIONAL RAC SERVICES

ADDITIONAL RAC SERVICES

Search Services

Retrospective Searches are conducted at a flat fee of $125 per search. If no references are identified, a $50 service charge will be made in lieu of the above. For best results, please call or write for assistance in formulating your search question. An extra charge, based on engineering time and costs, will be made for evaluating, extracting or summarizing information from the cited references.

Consulting Services

Consulting Service fees are determined by the costs incurred in the conduct of the designed work, including staff time and overhead, materials and other expenses. Work will be initiated upon receipt of a signed purchase order. We will be pleased to prepare firm cost proposals.

Full Service Participating Plans

Two plans are offered to both government and industry

Participating Member (PM)......................	**$1,600**
Participating Associate (PA)....................	**400**

Services provided to a Participant in either plan are:

- Automatic receipt of one (1) copy of each RAC microcircuit and semiconductor device databook issued over twelve months at a savings of $70.
- Availability of additional copies of each of the above databooks at 20% off list price.
- Discount on registration fees for RAC sponsored training courses, seminars, workshops, etc.

In addition, the **Participating Member** may access RAC resources as needed without issuing purchase orders. Up to 50 man-hours of professional consultation are authorized.

Blanket Purchase Order

The Blanket Purchase Order option enables you to write a single Purchase Order for a stipulated maximum dollar amount (depending on your needs) and active time duration (a one-year period is suggested), but you pay only for services rendered or documents purchased.

Military Agencies: Blanket Purchase Agreement, DD Form 1155, may be useful for ordering RAC reports and/or services. Please stipulate maximum dollar amount authorized and cutoff date on your order. Also specify services (e.g., publications, search services, etc.) to be provided. Identify vendor as IIT Research Institute (Reliability Analysis Center).

Ordering Information

Place orders or obtain additional information directly from the Reliability Analysis Center. Clearly specify the publications and services desired. Except for blanket purchase orders, prepayment is required. All foreign orders must be accompanied by a check drawn on a U.S. bank. Please make checks payable to IITRI/RAC.

SERVICE FEE SCHEDULE AND ORDERING INFORMATION

			Issue Date	Price Per Copy Domestic	Price Per Copy Foreign
Component Reliability Databooks					
( )	MDR-12	Digital Failure Rate Data	June 1979	$60.00	$70.00*
( )	MDR-13	Memory/LSI Data — Complete Set: $310	November 1979	60.00	70.00
( )	MDR-14	Hybrid Circuit Data — ($360 non U.S.)	March 1980	60.00	70.00*
( )	MDR-15	Digital Evaluation and Generic Failure Analysis Data - Vols. I and II	August 1980	60.00	70.00**
( )	MDR-16	Linear/Interface Data	January 1981	60.00	70.00*
( )	DSR-3	Transistor/Diode Data	January 1980	60.00	70.00**
( )	NPRD-1	Nonelectronic Parts Reliability Data	August 1978	60.00	70.00*
Equipment Databooks					
( )	EERD-1	Electronic Equipment Reliability Data	October 1980	60.00	70.00*
( )	EEMD-1	Electronic Equipment Maintainability Data	October 1980	60.00	70.00*
RAC Design Handbook					
( )	RDH-376	Reliability Design Handbook	March 1976	36.00	46.00**
Technical Reliability Studies					
( )	TRS-1	Microcircuit Screening Effectiveness		36.00	46.00*
( )	TRS-2	Search and Retrieval Index to IRPS Proceedings-1968 to 1978		24.00	34.00**
( )	TRS-3	EOS/ESD Technology Abstracts		36.00	46.00*
( )	TM 72-1	Microcircuit Wire Bond Reliability		24.00	34.00*
Symposium Proceedings					
( )	EOS-1	Electrical Overstress/Electrostatic Discharge 1979 Symposium Proceedings		24.00	34.00*
( )	EOS-2	Electrical Overstress/Electrostatic Discharge 1980 Symposium Proceedings		24.00	34.00*

***For air mail shipment to points outside North and Central America, add $7.50 per item**
****For air mail shipment to points outside North and Central America, add $12.50 per item**

Quantity Purchase Discounts - Discounts applicable to publications (for multiple copies of a single title order at one time) are:

Quantity	Discount	Quantity	Discount
1-2	list	10-19	33-1/3% off list
3-6	15% off list	20-49	45% off list
6-9	20% off list	50-99	60% off list
		100 or more	negotiable

ORDER FORM

Enclosed find $__________

Send order and check to:

Reliability Analysis Center
RADC/RBRAC
Griffiss AFB, NY 13441

Phone: 315/330-4151 Autovon: 587-4151

Please send me the documents checked above.

Name/Title______________________________

Organization____________________________

Address_________________________________

City/State______________________Zip______

Prepayment of orders is required. Please make checks payable to IITRI/RAC. Foreign orders must be accompanied by check drawn on a U.S. bank.

The Reliability Analysis Center is a DoD Information Analysis Center operated by IIT Research Institute, Chicago, IL

50272-101

REPORT DOCUMENTATION PAGE

1. REPORT NO.
TRS-3

2.

3. Recipient's Accession No.

4. Title and Subtitle

Technical Reliability Study
EOS/ESD Technology Abstracts

5. Report Date
Winter 80/81

6.

7. Author(s)
Wayne Grimaldi, Eugene Kraeger

8. Performing Organization Rept. No.

9. Performing Organization Name and Address

Reliability Analysis Center (RBRAC)
Rome Air Development Center
Griffiss Air Force Base, NY 13441

10. Project/Task/Work Unit No.

11. Contract(C) or Grant(G) No.
(C) F30602-78-C-0281
(G)

12. Sponsoring Organization Name and Address

Rome Air Development Center
Griffiss Air Force Base, NY 13441

13. Type of Report & Period Covered
N/A

14.

15. Supplementary Notes

This is one of a series of technical reliability studies.

16. Abstract (Limit: 200 words)

The EOS/ESD Technology Abstracts is a bibliography which references literature pertinent to Electrical Overstress and Electrostatic Discharge damage or degradation of electronic devices. The purpose of this bibliography is to make more accessible present information on Electrical Overstress and Electrostatic Discharge aspects such as design, failure analysis, protective measures and techniques, and training programs. Duplication of previous studies can be avoided by the increased information retrieval capability provided by this bibliography.

17. Document Analysis a. Descriptors

b. Identifiers/Open-Ended Terms

Electrical Overstress
Electrostatic Discharge
Component Damage
Failure Analysis
Protective Measures

c. COSATI Field/Group

18. Availability Statement
Approved for public release; distribution unlimited. Available from RAC or NTIS.

19. Security Class (This Report)
Unclassified

20. Security Class (This Page)
Unclassified

21. No. of Pages
151

22. Price
$36.00

(See ANSI-Z39.18) See Instructions on Reverse OPTIONAL FORM 272 (4-77) (Formerly NTIS-35) Department of Commerce